8085 PIN DESCRIPTION

- READY: This an output signal used to check the status of output device. If it is low, µP will WAIT until it is high.

- TRAP: It is an Edge triggered highest priority, non mask able interrupt. After TRAP, restart occurs and execution starts from address 0024H.

- RST5.5,6.5,7.5: These are maskable interrupts and have low priority than TRAP.

- INTR^- &INTA: INTR is a interrupt request signal after which µP generates INTA or interrupt acknowledge signal.

- IO/M^-: This is output pin or signal used to indicate whether 8085 is working in I/O mode(IO/M^-=1) or Memory mode(IO/M^-=0).
Arithmetic and Logical group

Accumulator: It is 8-bit general purpose register.
• It is connected to ALU.
• So most of the operations are done in Acc.

Temporary register: It is not available for user
• All the arithmetic and logical operations are done in the temporary register but user can’t access it.

Flag: It is a group of 5 flip flops used to know status of various operations done.
• The Flag Register along with Accumulator is called PSW or Program Status Word.
Register Group

- **Temporary registers (W,Z):** These are not available for user. These are loaded only when there is an operation being performed.

- **General purpose:** There are six general purpose registers in 8085 namely B,C,D,E,H,L. These are used for various data manipulations.

- **Special purpose:** There are two special purpose registers in 8085:
  1. **SP:** Stack Pointer.
  2. **PC:** Program Counter.
Register Group

Stack Pointer: This is a temporary storage memory 16 bit register. Since there are only 6 general purpose registers, there is a need to reuse them.

- Whenever stack is to be used previous values are PUSHED on stack and then after the program is over these values are POPED back.

Program Counter: It is 16 bit register used to point the location from which the next instruction is to be fetched.

- When a single byte instruction is executed PC is automatically incremented by 1.
- Upon reset PC contents are set to 0000H and next instruction is fetched onwards.
INTERRUPT CONTROL

• It accepts different interrupts like TRAP INT5.5,6.5,7.5 and INTR.

SERIAL IO CONTROL GROUP

• It is used to accept the serial 1 bit data by using SID and SOD signals and it can be performed by using SIM & RIM instructions.
LOGICAL GROUP

RLC (Rotate accumulator left).

Example:
MOV A,03H.

RLC (Rotate accumulator left).

Initially

A=03H

After execution

A=06H.

Flags Affected: Only carry flag is affected.

Addressing mode: Implied.
Write a program to reset last 4 bits of the number 32H. Store result at C200H.

MVI A, 32H  
A=32H

ANI F0H  
00110010 AND

11110000  
=00110000=30H

STA C200H.  
C200=30H

RST1  
Stop
STACK AND MACHINE CONTROL

POP Rp (Pop register pair contents from stack).  
Example: POP D (POP the content of DE pair from Stack).

• Suppose at DE pair the data is H= 20H, L= 30H SP was initialized at FFFFH

Initially                                             After execution
D=20H, E=30H                                 D=10H, E=80H.
FFFD=80H, FFFE=10H    
Flags Affected : No flags affected.    
Addressing mode: Register indirect
ADDRESSING MODES OF 8085

Implied addressing:
• These doesn’t require any operand. The data is specified in Opcode itself.

Example: RAL: Rotate left with carry.

No.of Bytes:
These are single byte instruction or Opcode only.
Write a program to transfer a block of data from C550H to C55FH. Store the data from C570H to C57FH.

LXI H, C550H
LXI B, C570H
MVI D, 0FH
UP MOV A, M
STAX B
INX H
INX B
DCR D
JNZ UP
RST1
• In this example we saw that some address lines are used for interfacing while others are for decoding.

• It is called absolute decoding.

• We sometimes don’t require that many address lines. So we ignore them. But this may lead to shadowing or multiple address.

• This type of decoding is called linear decoding or partial decoding.

• In partial decoding, wastage of address takes place but it requires less hardware and cost is also less as compared with absolute one.
Figure 1. 82C55A Block Diagram
A\textsubscript{0}, A\textsubscript{1} decide the port to be used in 8255.

<table>
<thead>
<tr>
<th>A\textsubscript{1}</th>
<th>A\textsubscript{0}</th>
<th>Selected port</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Port A</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Port B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Port C</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Control Register</td>
</tr>
</tbody>
</table>
8255 MODES

- **Mode 0**: Simple I/O
  - Any of A, B, CL and CH can be programmed as input or output
- **Mode 1**: I/O with Handshake
  - A and B can be used for I/O
  - C provides the handshake signals
- **Mode 2**: Bi-directional with handshake
  - A is bi-directional with C providing handshake signals
  - B is simple I/O (mode-0) or handshake I/O (mode-1)
- **BSR (Bit Set Reset) Mode**
  - Only C is available for bit mode access.
  - Allows single bit manipulation for control applications
Full Duplex: It is a two way communication between two ports and both parties can communicate at the same time.

- Thus here efficient communication can be established.
Interrupts In 8085

- Interrupt is a process where an external device can get the attention of the microprocessor.
  - The process starts from the I/O device
  - The process is asynchronous.

- **Classification of Interrupts**
  - **Maskable Interrupts** (Can be delayed or Rejected)
  - **Non-Maskable Interrupts** (Cannot be delayed or Rejected)
## INTERRUPT PRIORITY

<table>
<thead>
<tr>
<th>Interrupt name</th>
<th>Mask-able</th>
<th>Vectored</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRAP</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>RST 7.5</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>RST 6.5</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>RST 5.5</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>INTR</td>
<td>YES</td>
<td>NO</td>
</tr>
</tbody>
</table>
SIM INSTRUCTION

- Example: Set the interrupt masks so that RST5.5 is enabled, RST6.5 is masked, and RST7.5 is enabled.

- First, determine the contents of the accumulator.
  - Enable 5.5  bit 0 = 0
  - Disable 6.5  bit 1 = 1
  - Enable 7.5  bit 2 = 0
  - Allow setting the masks  bit 3 = 1
  - Don’t reset the flip flop  bit 4 = 0
  - Bit 5 is not used  bit 5 = 0
  - Don’t use serial data  bit 6 = 0
  - Serial data is ignored  bit 7 = 0

\[
\begin{array}{cccccccc}
\text{SDO} & \text{SDE} & \text{XXX} & \text{R7.5} & \text{MSE} & \text{M7.5} & \text{M6.5} & \text{M5.5} \\
0 & 0 & 0 & 0 & 1 & 0 & 1 & 0 \\
\end{array}
\]

- EI  ; Enable interrupts including INTR
- MVI A, 0A  ; Prepare the mask to enable RST 7.5, and 5.5, disable 6.5
- SIM  ; Apply the settings RST masks