SECTION 1
BASIC LINEAR REGULATOR THEORY

A. IC Voltage Regulator

The basic functional block diagram of an integrated circuit voltage regulator is shown in Figure 1–1. It consists of a stable reference, whose output voltage is V_{ref}, and a high gain error amplifier. The output voltage (V_O), is equal to or a multiple of V_{ref}. The regulator will tend to keep V_O constant by sensing any changes in V_O and trying to return it to its original value. Therefore, the ideal voltage regulator could be considered a voltage source with a constant output voltage. However, in practice the IC regulator is better represented by the model shown in Figure 1–2.

In this figure, the regulator is modeled as a voltage source with a positive output impedance (Z_O). The value of the voltage source (V) is not constant; instead it varies with changes in supply voltage (V_{CC}) and with changes in IC junction temperature (T_J) induced by changes in ambient temperature and power dissipation. Also, the regulator output voltage (V_O) is affected by the voltage drop across Z_O, caused by the output current (I_O). In the following text, the reference and amplifier sections will be described, and their contributions to the changes in the output voltage analyzed.

B. Voltage Reference

Naturally, the major requirement for the reference is that it be stable; variations in supply voltage or junction temperature should have little or no effect on the value of the reference voltage (V_{ref}).

1. Zener Diode Reference

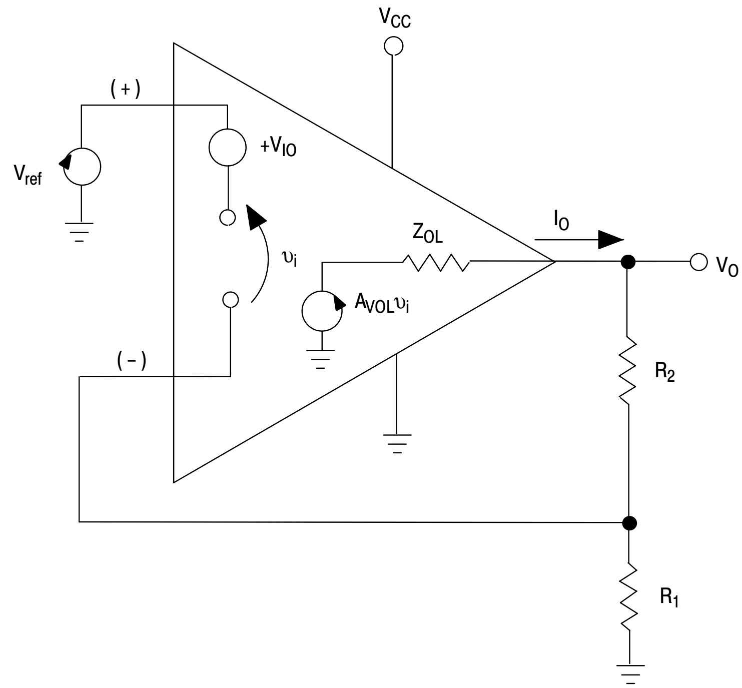
The simplest form of a voltage reference is shown in Figure 1–3a. It consists of a resistor and a zener diode. The zener voltage (V_Z) is used as the reference voltage. In order to determine V_Z, consider Figure 1–3b. The zener diode (VR1) of Figure 1–3a has been replaced with its equivalent circuit model and the value of V_Z is therefore given by (at a constant junction temperature):

$$V_Z = V_{BZ} + I_Z Z_Z = V_{BZ} + \left(\frac{V_{CC} - V_{BZ}}{R + Z_z}\right) Z_Z \tag{1}$$

where: V_{BZ} = zener breakdown voltage
I_Z = zener current
Z_Z = zener impedance at I_Z.

Note that changes in the supply voltage give rise to changes in the zener current, thereby changing the value of the reference voltage (V_Z).

Figure 1–6. Typical Voltage Regulator Configuration



The definition of common mode voltage (V_{CM}), illustrated by Figure 1–7(a), is

$$V_{CM} = \left[\frac{V_1 + V_2}{2}\right] - \left[\frac{(V+) + (V-)}{2}\right] \tag{12}$$

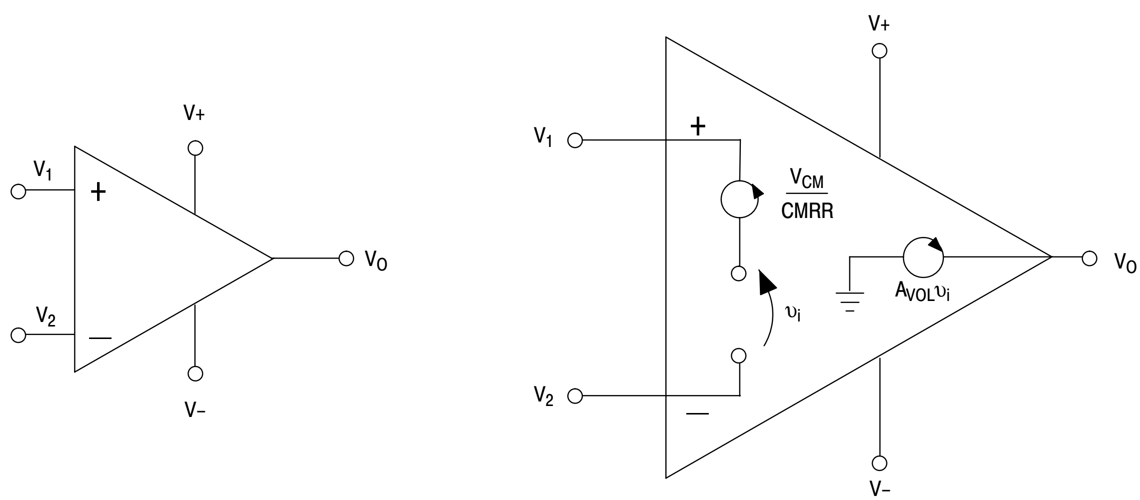
where: V_1 = voltage on amplifier noninverting input

V_2 = voltage on amplifier inverting input

V+ = positive supply voltage

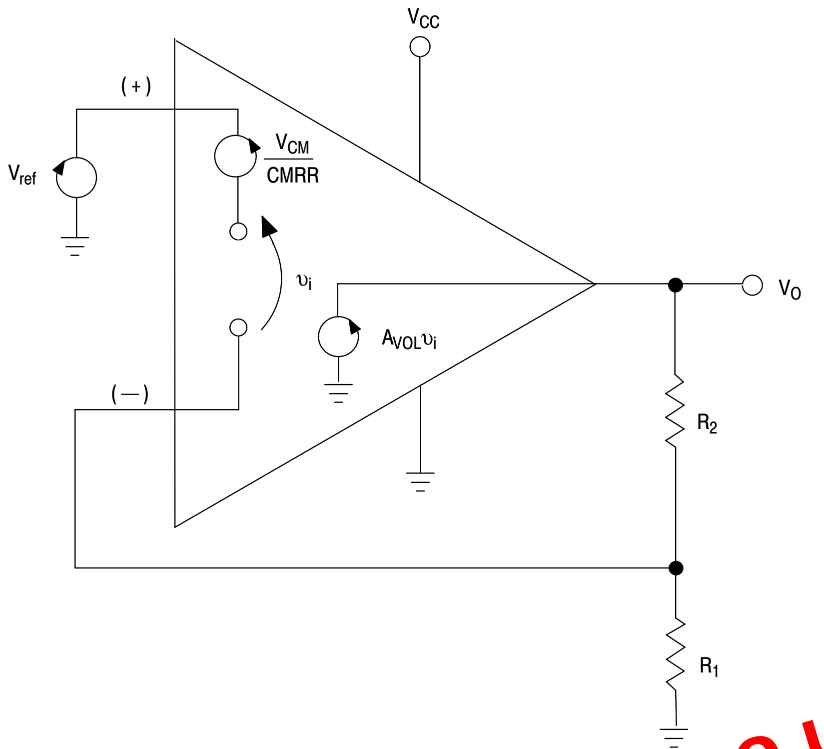
V– = negative supply voltage

Figure 1–7. Definition of Common Mode Voltage Error



(a) **(b)**

Figure 1–8. Common Mode Regulator Effects



In an ideal amplifier, only the differential input voltage (V_1 – V_2) has any effect on the output voltage; the value of V_{CM} would not effect the output. In fact, V_{CM} does influence the amplifier output voltage. This effect can be modeled as an additional voltage offset at the amplifier input equal to V_{CM}/CMRR as shown in Figures 1–7 and 1–8. The latter figure is the same configuration as Figure 1–6, with amplifier input offset voltage and output impedance deleted for clarity and common mode voltage effects added. The output voltage of this configuration is given by:

$$V_O = A_{VOL}\,\upsilon_i = A_{VOL}\left(V_{ref} - \frac{V_{CM}}{CMRR} - \beta V_O\right) \tag{13}$$

Manipulating,

$$V_O = \frac{\left(V_{ref} - \frac{V_{CM}}{CMRR}\right)}{\beta + \frac{1}{A_{VOL}}} \tag{14}$$

where: $$V_{CM} = V_{ref} - \frac{V_{CC}}{2} \tag{15}$$

and, CMRR = common mode rejection ratio

It can be seen from Equations (14) and (15) that the output can vary when V_{CC} varies. This can be reduced by designing the amplifier to have a high A_{VOL}, a high CMRR, and by choosing the feedback ratio (β) to be unity.

SECTION 2

SELECTING A LINEAR IC VOLTAGE REGULATOR

A. Selecting the Type of Regulator

There are five basic linear regulator types; positive, negative, fixed output, tracking and floating regulators. Each has its own particular characteristics and best uses, and selection depends on the designer's needs and trade–offs in performance and cost.

1. Positive Versus Negative Regulators

In most cases, a positive regulator is used to regulate positive voltages and a negative regulator negative voltages. However, depending on the system's grounding requirements, each regulator type may be used to regulate the "opposite" voltage.

Figures 2–1a and 2–1b show the regulators used in the conventional and obvious mode. Note that the ground reference for each (indicated by the heavy line) is continuous. Several positive regulators could be used with the same input supply to deliver several voltages with common grounds; negative regulators may be utilized in a similar manner.

If no other common supplies or system components operate off the input supply to the regulator, the circuits of Figures 2–1c and 2–1d may be used to regulate positive voltages with a negative regulator and vice versa. In these configurations, the input supply is essentially floated, i.e., neither side of the input is tied to the system ground.

There are methods of utilizing positive regulators to obtain negative output voltages without sacrificing ground bus continuity. However, these methods are only possible at the expense of increased circuit complexity and cost. An example of this technique is shown in Section 3.

2. Three–Terminal, Fixed Output Regulators

These regulators offer the designer a simple, inexpensive way to obtain a source of regulated voltage. They are available in a variety of positive or negative output voltages and current ranges.

The advantages of these regulators are:

a) Easy to use.
b) Internal overcurrent and thermal protection.
c) No circuit adjustments necessary.
d) Low cost.

Their disadvantages are:

a) Output voltage cannot be precisely adjusted. (Methods for obtaining adjustable outputs are shown in Section 3).
b) Available only in certain output voltages and currents.
c) Obtaining greater current capability is more difficult than with other regulators. (Methods for obtaining greater output currents are shown in Section 3.)

4. Reverse Bias Protection

Occasionally, there exists the possibility that the input voltage to the regulator can collapse faster than the output voltage. This could occur, for example, if the input supply is “crowbarred” during an output overvoltage condition. If the output voltage is greater ≈ 7.0 V, the emitter–base junction of the series pass element (internal or external) could break down and be damaged. To prevent this, a diode shunt can be employed, as shown in Figure 3–2F.

Figure 3–3F shows a three–terminal positive–adjustable regulator with the recommended protection diodes for output voltages in excess of 25 V, or high output capacitance values (C_O > 25 μF, C_{Adj} >10 μF). Diode D1 prevents C_O from discharging through the regulator during an input short circuit. Diode D2 protects against capacitor C_{Adj} from discharging through the regulator during an output short circuit. The combination of diodes D1 and D2 prevents C_{Adj} from discharging through the regulator during an input short circuit.

Figure 3–2F. Reverse Bias Protection

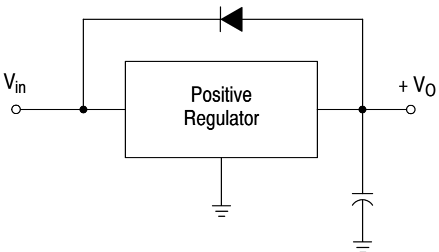


Figure 3–3F. Reverse Bias Protection for Three–Terminal Adjustable Regulators

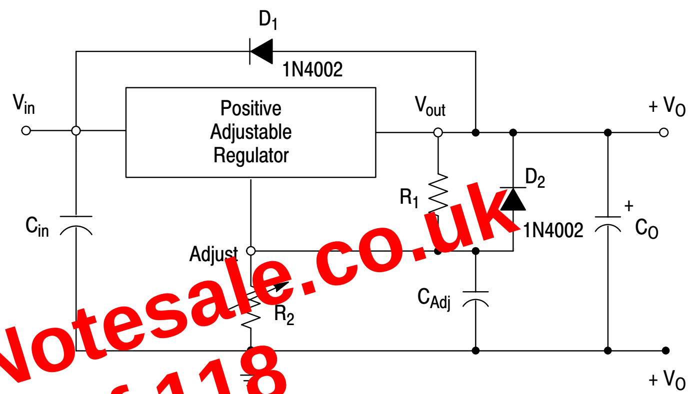


Figure 4–2. 2N3055 Safe Operating Area (SOA)

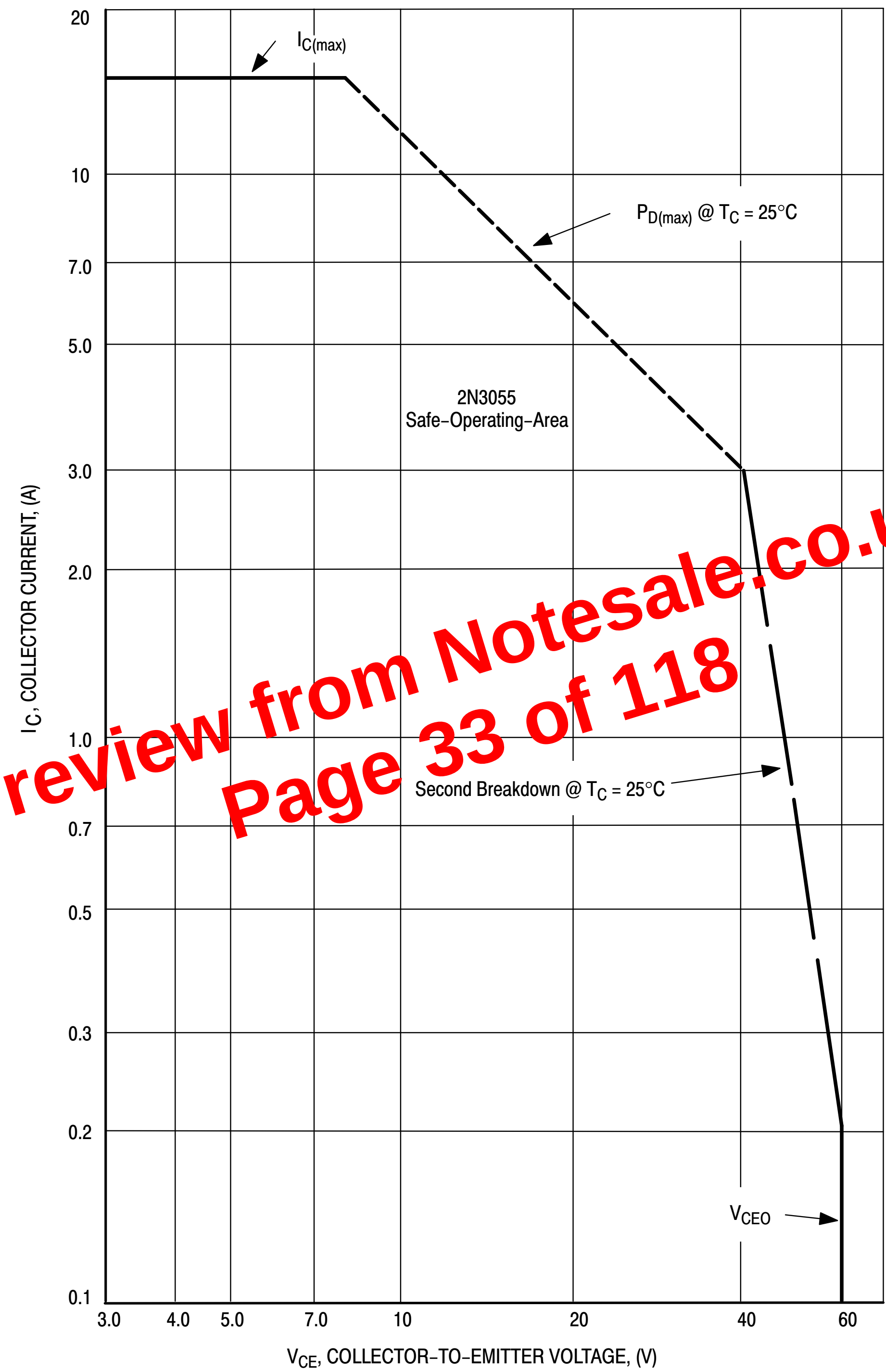
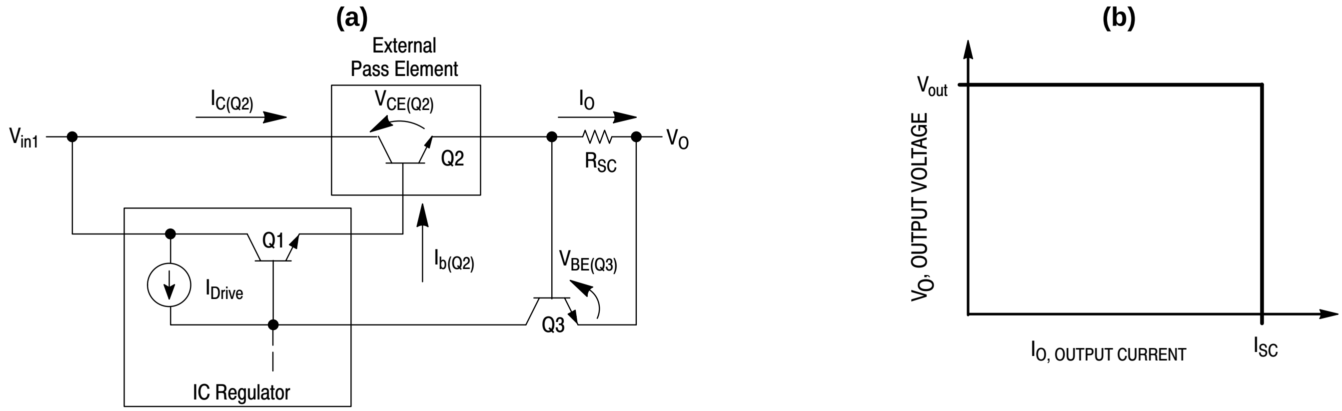


Figure 4–3. Constant Current Limiting



By using the base of Q1 in the IC regulator as a control point, this configuration has the added benefit of limiting the IC regulator output current ($I_{B(Q2)}$) to $Isc/h_{fe(Q2)}$, as well as limiting the collector current of Q2 to I_{SC}. Of course, access to this point is necessary. Fortunately, it is usually available in the form of a separate pin or as the regulator's compensation terminal.(1)

The required safe–operating–area for Q2 can be obtained by plotting the V_{CE} and I_C of Q2 given by:

$$V_{CE(Q2)} = V_{in1} - V_O - I_O R_{SC} \simeq V_{in1} - V_O \quad (4.8)$$

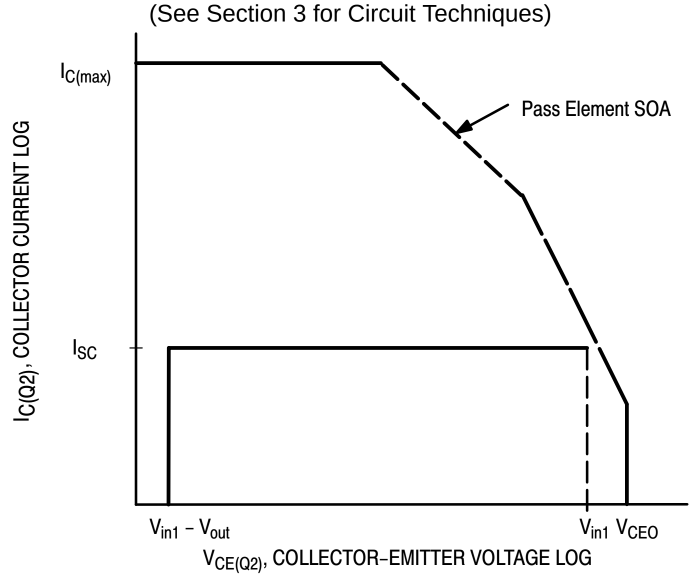
$$I_{C(Q2)} \simeq I_O \quad (4.9)$$

$$\text{where, } V_O = V_{out} \text{ for } 0 \leq I_O \leq I_{SC} \quad (4.10)$$

$$\text{and, } I_O = I_{SC} \text{ for } 0 \leq V_O \leq V_{out} \quad (4.11)$$

The resulting plot is shown in Figure 4–4. The transistor chosen for Q2 must have an SOA which encloses this plot, see Figure 4–4. Note that the greatest demand on the transistor's SOA capability occurs when the output of the regulator is short circuited and the pass element must support the full input voltage and short circuit current simultaneously.

Figure 4–4. Constant Current Limit SOA Requirements
(See Section 3 for Circuit Techniques)



(1) The three–terminal regulators have internal current limiting and therefore do not provide access to this point. If an external pass element is used with these regulators, constant current limiting can still be accomplished by diverting pass element drive.

2. Foldback Current Limiting

A disadvantage of the constant current limit technique is that in order to obtain sufficient SOA the pass element must have a much greater collector current capability than is actually needed. If the short circuit current could be reduced, while still allowing full output current to be obtained during normal regulator operation, more efficient utilization of the pass elements SOA capability would result. This can be done by using a “foldback” current limiting technique instead of constant current limiting.

The basic circuit configuration for this method is shown in Figure 4–5(A). The circuit operates in a manner similar to that of the constant current limiting circuit, in that output current control is obtained by diverting base drive away from Q1 with Q3.

At low output currents, V_A approximately equals V_O and V_{R2} is less than than V_O. Q3 is therefore non–conducting and the output voltage remains constant. As the output current increases, the voltage drop across R_{SC} increases until V_A and V_{R2} are great enough to bias Q3 on. The output current at which this occurs is I_K, the “knee” current.

Figure 4–5. Foldback Current Limiting

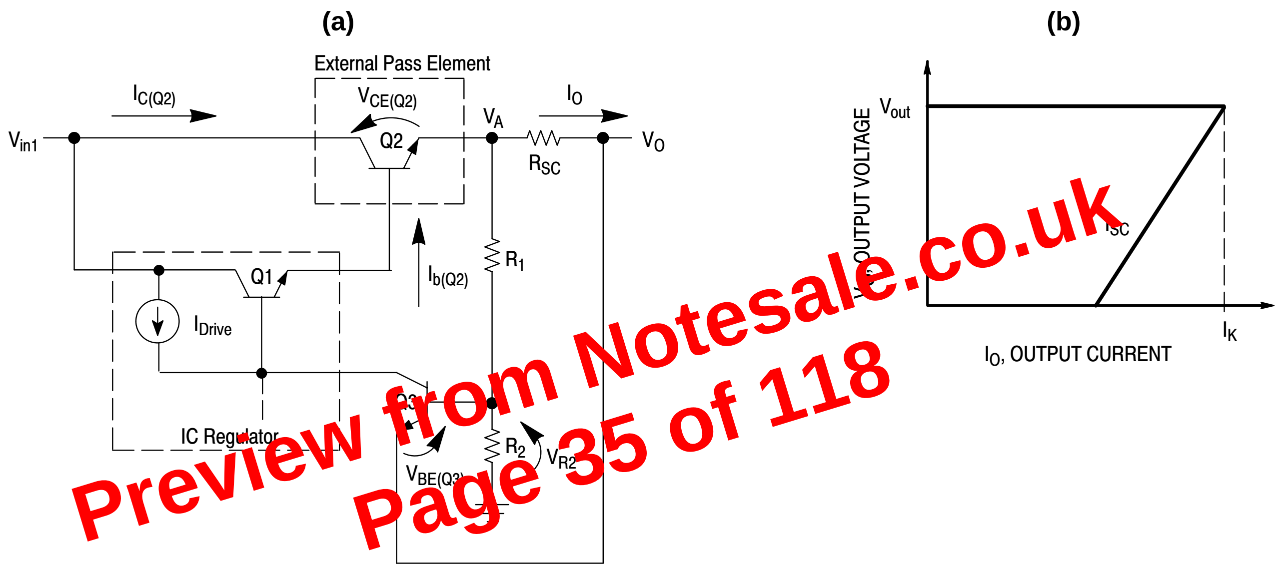
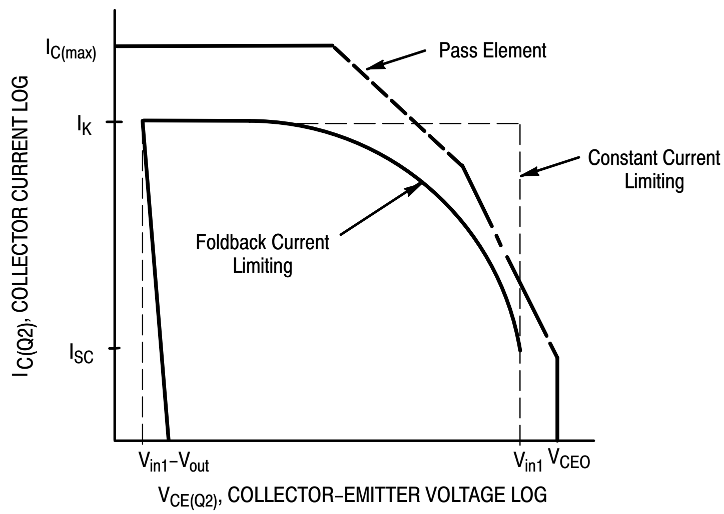


Figure 4–6. Foldback Current Limit SOA Requirements



SECTION 5

LINEAR REGULATOR CONSTRUCTION AND LAYOUT

An important, and often neglected, aspect of the total regulator circuit design is the actual layout and component placement of the circuit. In order to obtain excellent transient response performance, high frequency transistors are used in modern integrated circuit voltage regulators. Proper attention to circuit layout is therefore necessary to prevent regulator instability or oscillations, or degraded performance.

In this section, guidelines will be given on proper regulator layout and placement of circuit components. In addition, topics such as remote voltage sensing, semiconductor mounting techniques, and thermal system evaluations will also be discussed.

1. General Layout and Component Placement Considerations

As mentioned previously, modern integrated circuit regulators are necessarily high bandwidth devices in order to obtain good transient response characteristics. To insure stable closed–loop operation, all these devices are frequency compensated, either internally or externally. This compensation can easily be upset by unwanted stray circuit capacitances and lead inductances, resulting in spurious oscillations. Therefore, it is important that the circuit lead lengths be short and the layout as tight as possible. Particular attention should be paid to locating the compensation and bypass capacitors as close to the IC as possible. Lead lengths associated with the external pass element(s), if used, should also be minimized.

Often overlooked is the stray inductance associated with the input leads to the regulator circuit. If the lead length from the input supply filter capacitor to the regulator input is more than a couple of inches, a 0.01 μF to 1.0 μF high frequency type capacitor (tantalum, ceramic, etc.) should be used to bypass the supply leads close to the regulator input pins.

2. Ground Loops and Remote Voltage Sensing

Ground Loops — Regulator performance can also suffer if ground loops in the circuit wiring are not avoided. The most common ground loop problem occurs when the return lead of the input supply filter capacitor is improperly located, as shown in Figure 5–1. If this return lead is physically connected between the load return and the regulator circuit ground point (“B”), a ripple voltage component (60 Hz or 120 Hz) can be induced on the load voltage (V_L). This is due to the high peaks of the filter capacitor ripple current (I_{ripple}) flowing through the lead resistance between the load and regulator. These peaks can be 5 to 15 times the value of load current. Since the regulator will only keep constant the voltage between its sense lead and ground point, points “A” and “B” in Figure 5–1, this additional ripple voltage (V_{lead}), will appear at the load.

This problem can be avoided by proper placement and connection of the filter capacitor return load as shown in Figure 5–2.

Remote Voltage Sensing — Closely related to the above ground loop problem is resistance in the current carrying leads to the load. This can cause poorer than expected load regulation in cases where the load currents are large or where the load is located some distance from the regulator. This is illustrated in Figure 5–3. As stated previously, the regulator circuit will keep the voltage present between its sense and ground pins constant. From Figure 5–3 we can see that any lead resistance between these points and the load will cause the load voltage (V_L) to vary with varying load current, I_L. This effectively lowers the load regulation of the circuit.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 μin. to 60 μin. is satisfactory. A finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy using a copper TO–204 (TO–3) package with a typical 32 μin. finish, showed that heatsink finishes between 16 μin. and 64 μin. caused less than ±2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.[3] Most commercially available cast or extruded heatsinks will require spotfacing when used in high power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO–204AA, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This “crater” in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat–dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early–life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine–edge blanking or sheared–through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four–post die sets equipped with proper pressure pads and holding fixtures.

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black–anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromate–acid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of the paint’s high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 V.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

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(3) Catalog #87–HS–9 (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381–0839.

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho–Therm 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R\theta_{CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in–lb from an initial 6 in–lb. With non–conformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Table 5–3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 5–3. Performance of Silicon Rubber Insulators Tested per MIL–I–49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data(1)	Bergquist Data(2)
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	—
Cho–Therm, 1617	0.233	—
Q Pad (non–insulated)	—	0.009
Sil–Pad, K–10	0.263	0.200
Thermasil III	0.267	—
Mica, greased	0.329	0.400
Sil–Pad 1000	0.400	0.300
Cho–therm 1674	0.433	—
Thermasil II	0.500	—
Sil–Pad 400	0.533	0.440
Sil–Pad K–4	0.583	0.440

(1) From Thermalloy EIR 87–1030
(2) From Bergquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly, so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi–pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost–effective insulated packages since the 1950s. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The second category contains parts which have a plastic overmold covering the metal mounting base. The Full Pak (Case 221C) illustrated in Figure 5–13, is an example of parts in the second category.

Appendix A
Thermal Resistance Concepts

The basic equation for heat transfer under steady–state conditions is generally written as:

$$q = hA\Delta T \tag{1}$$

where, q = rate of heat transfer or power dissipation (P_D),
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

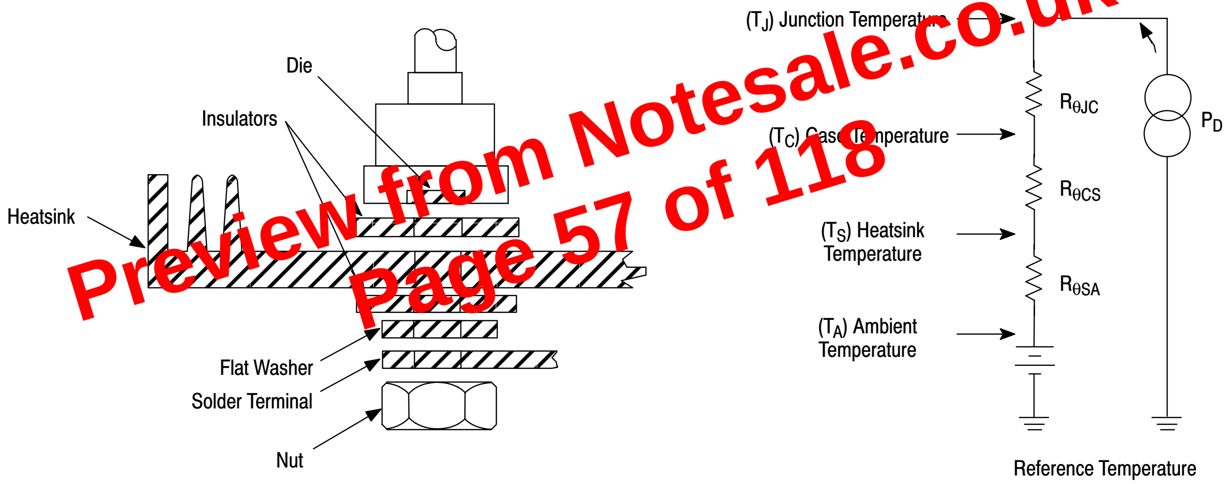
However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance (R_θ) is

$$R_\theta = \Delta T/q = 1/hA \tag{2}$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation 2 and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure A–1.

Figure A–1. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor



The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

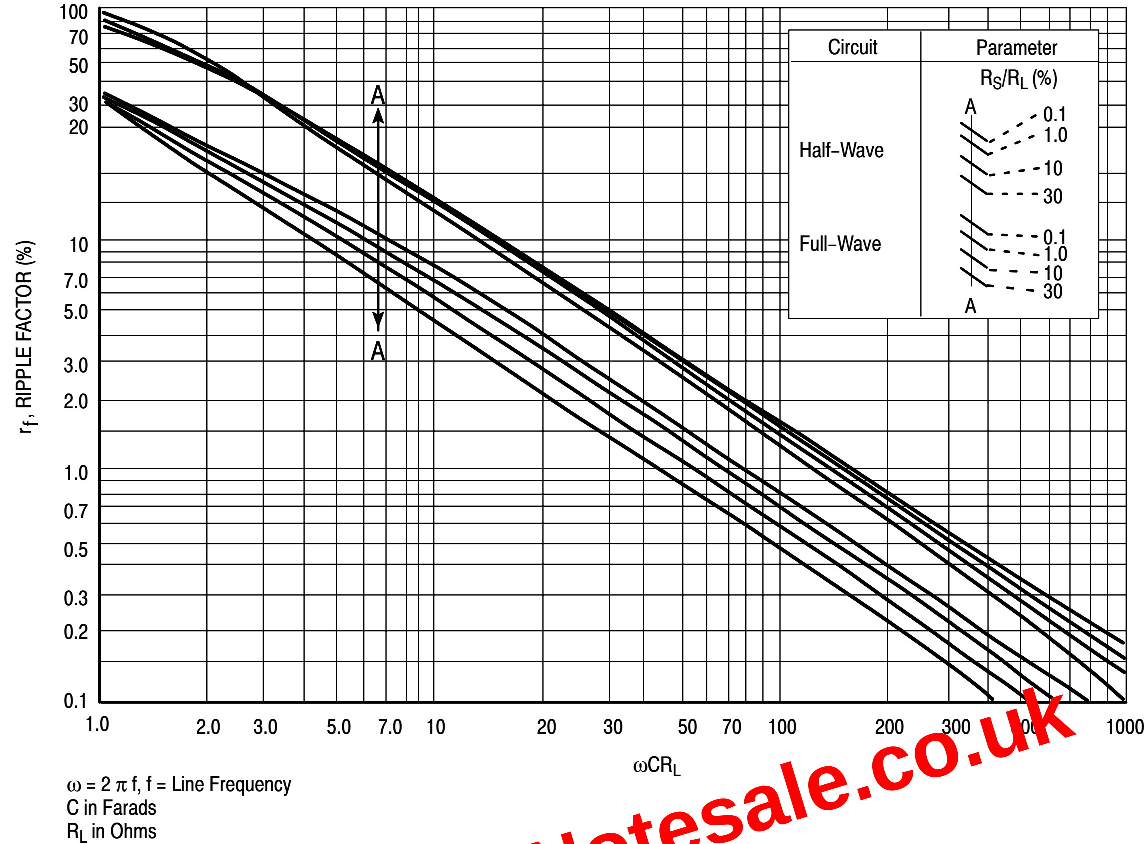
$$T_J = P_D(R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) + T_A \tag{3}$$

where, T_J = junction temperature,
P_D = power dissipation,
$R_{\theta JC}$ = semiconductor thermal resistance (junction–to–case),
$R_{\theta CS}$ = interface thermal resistance (case–to–heatsink),
$R_{\theta SA}$ = heatsink thermal resistance (heatsink–to–ambient),
T_A = ambient temperature.

The thermal resistance junction–to–ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance ($R_{\theta CS}$) may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

Figure 8–5. Root–Mean–Square Ripple Voltage for Capacitor–Input Circuits



Returning to the above curves, the full–wave circuit will be considered. Figure 8–3 shows that a circuit must operate with $\omega CR_L \geq 10$ in order to hold the voltage reduction to less than 10% and $\omega CR_L \geq 40$ to obtain less than 5.0% reduction. However, it will also be seen that these voltage reduction figures require R_S/R_L, where R_S is now the total series resistance, to be about 0.1% which, if attainable, causes repetitive peak–to–average current ratios from 10 to 17 respectively, as can be seen from Figure 8–4. These ratios can be satisfied by many diodes; however, they may not be able to tolerate the turn–on surge current generated when the input–filter capacitor is discharged and the transformer primary is energized at the peak of the input waveform. The rectifier is then required to pass a surge current determined by the peak secondary voltage less the rectifier forward drop and limited only by the series resistance R_S. In order to control this turn–on surge, additional resistance must often be provided in series with each rectifier. It becomes evident, then, that a compromise must be made between voltage reduction on the one hand and diode surge rating and hence average current–carrying capacity on the other hand. If small voltage reduction, that is good voltage regulation, is required, a much larger diode is necessary than that demanded by the average current rating.

Surge Current

The capacitor–input filter allows a large surge to develop, because the reactance of the transformer leakage inductance is rather small. The maximum instantaneous surge current is approximately V_M/R_S and the capacitor charges with a time constant $\tau \approx R_S C_1$. As a rough — but conservative — check, the surge will not damage the diode if V_M/R_S is less than the diode I_{FSM} rating and τ is less than 8.3 ms. It is wise to make R_S as large as possible and not pursue tight voltage regulation; therefore, not only will the surge be reduced but rectifier and transformer ratings will more nearly approach the DC power requirements of the supply.

Most switchmode transistor load lines are inductive during turn–on and turn–off. Turn–on is generally inductive because the short circuit created by output rectifier reverse recovery times is isolated by leakage inductance in the transformer. This inductance effectively snubs most turn–on load lines so that the rectifier recovery (or short circuit) current and the input voltage are not applied simultaneously to the transistor. Sometimes primary interwinding capacitance presents a small current spike but usually turn–on transients are not a problem. Turn–off transients due to this same leakage inductance, however, are almost always a problem. In bridge circuits, clamp diodes can be used to limit these voltage spikes. If the resulting inductive load line exceeds the transistor's reverse bias switching capability (RBSOA) then an RC network may also be added across the primary to absorb some of this transient energy. The time constant of this network should equal the anticipated switching time of the transistor (50 ns to 500 ns). Resistance values of 100 Ω to 1000 Ω in this RC network are generally appropriate. Trial and error will indicate how low the resistor has to be to provide the correct amount of snubbing. For single transistor converters, the circuits shown in Figure 11–1 are generally used.

Here slightly different criteria are used to define the R and C snubber values:

$$C = \frac{I\,t_f}{V}$$

where; I = the peak switching current

t_f = the transistor fall time

V = the peak switching voltage (Approximately twice the DC bus)

also, R = t_{on}/C (it is not necessary to completely discharge this capacitor in order to obtain the desired effects of this circuit)

where, t_{on} = the minimum on–time or pulse width

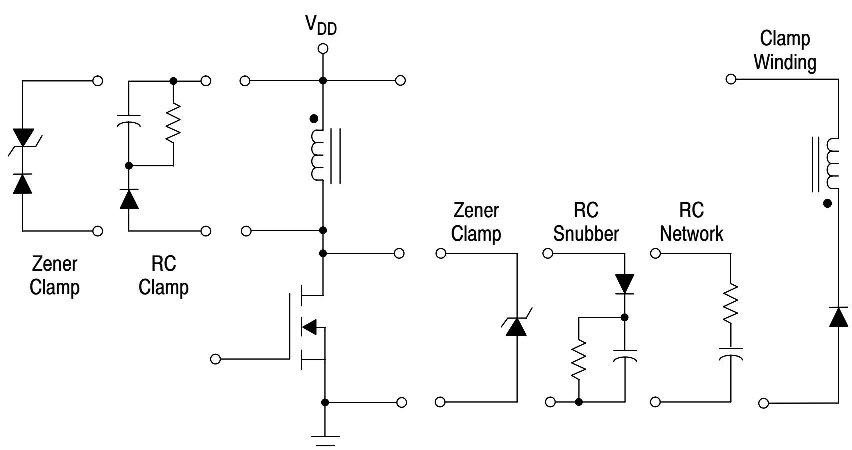
and, $$P_R = \frac{CV^2f}{2}$$

where, P_R = the power rating of the resistor

and, f = the operating frequency.

In most of today's designs snubber elements are small or nonexistent and voltage spikes from energy left in the leakage inductance is a more critical problem depending on how good the coupling is between the primary and clamp windings and how fast the clamp diode turns on. FETs often have to be slowed down to prevent self destruction from this spike.

Figure 11–1. Protection Circuits for Switching Transistors



Half and Full–Bridge

The most popular high power converter is the half–bridge (Figure 12–6). It has two clear advantages over the push–pull and became the favorite rather quickly. First, the transistors never see more than the peak line voltage and the standard 400 V fast switchmode transistors that are readily available may be used. And second, and probably even more important, transformer saturation problems are easily minimized by use of a small coupling capacitor (about 2.0 μF to 5.0 μF) as shown above. Because the primary winding is driven in both directions, a full–wave output filter, rather than half, is now used and the core is actually utilized more effectively. Another more subtle advantage of this circuit is that the input filter capacitors are placed in series across the rectified 220 V line which allows them to be used as the voltage doubler elements on a 120 V line. This still allows the inverter transformer to operate from a nominal 320 V bus when the circuit is connected to either 120 V or 220 V. Finally, this topology allows diode clamps across each transistor to contain destructive switching transients. The designer's dream, of course, is for fast transistors that can handle a clamped inductive load line at rated current. And a few (like the MJE16000 series from ON Semiconductor) are beginning to appear on the market. With the improved RBSOA that these transistors feature, less snubbing is required and this improves both the cost and efficiency of these designs.

Figure 12–5. Half–Bridge Converter with Split Windings

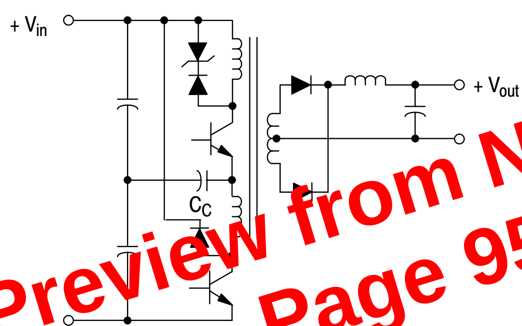
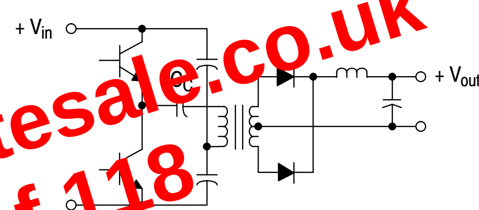


Figure 12–6. Half–Bridge Converter (200 W to 1.0 kW)



Basic Full–Bridge Configuration

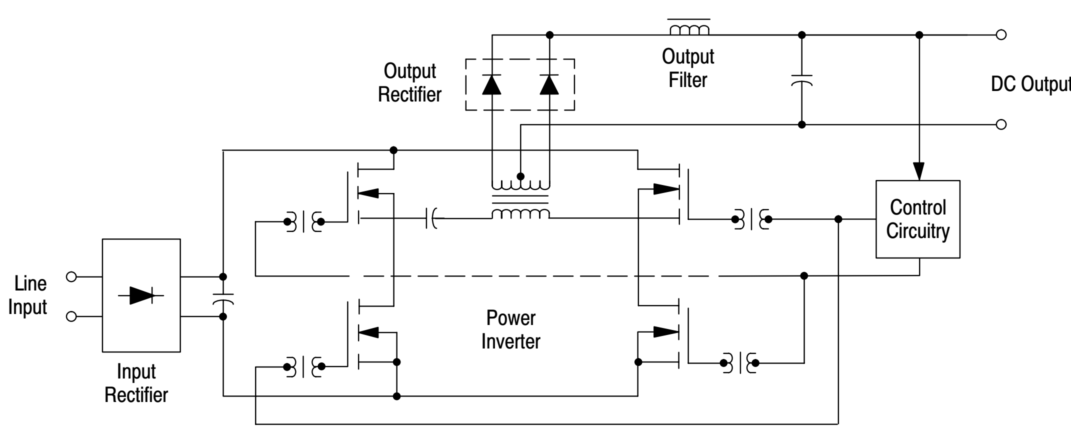


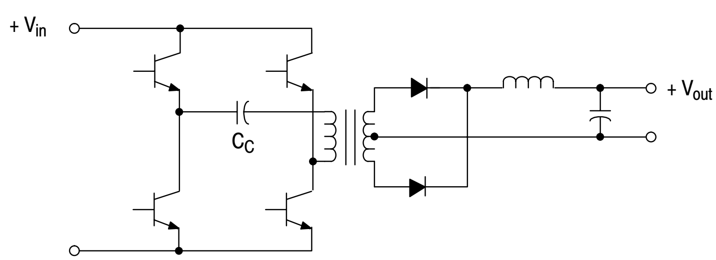
Table 12–4. Full–Bridge Semiconductor Selection Chart

Output Power	500 W		750 W		1000 W	
Input Voltage (V_{in})	120 V	220 V 240 V	120 V	220 V 240 V	120 V	220 V 240 V
MOSFET Requirements: Max Working Curren (I_W) Max Working Voltage (V_W)	5.7 A 190 V	3.1 A 380 V	8.6 A 190 V	4.7 A 380 V	11.5 A 190 V	6.25 A 380 V
Power MOSFETs Recommended: Metal (TO–204AA) (TO–3) Plastic (TO–220AB) Plastic (TO–218AC)	MTM8N20 MTP8N20 —	MTM4N45 MTP4N45 —	MTM10N25 MTP10N25 —	MTM7N45 MTP4N45 MTH7N45	MTM15N20 MTP12N20 MTH15N20	MTM7N45 — MTH7N45
Input Rectifiers: Max Working Current (I_W) Recommended Types	4.6 A MDA3506	2.5 A MDA3510	7.0 A	3.8 A	9.25 A	5.0 A
Output Rectifiers: Recommended types for output voltage of: 5.0 V 10 V 20 V 50 V 100 V	MBR20035CT MUR10010CT MUR10015CT MUR3015PT MUR804PT		MBR30035CT MUR10010CT* MUR10015CT MUR3015PT* MUR3040PT		MBR30035CT* MUR10010CT* MUR10015CT* MUR10015CT MUR3040PT	
Recommended Control Circuits	SG1525A, SG1526, TL494 Inverter Control Circuit MC3423 Overvoltage Detector Error Amplifier: Single TL431; Dual–LM358 Quad MC3403, LM324, LM2902					

*More than one device per leg, matched.

The effective current limit of today's low cost TO–218 discrete transistors (250 mil die) is somewhere in the 10 A to 20 A area. Once this limit is reached, the designer generally changes to the full–bridge configurations shown in Figure 12–7. Because full line rather than half is applied to the primary winding, the power out can be almost double that of the half–bridge with the same switching transistors. Power Darlington transistors are a logical choice for higher power control with current, voltage and speed capabilities allowing very high performance and cost effective designs. Another variation of the half–bridge is the split winding circuit, shown in Figure 12–5. A diode clamp can protect the lower transistor but a snubber or zener clamp must still be used to protect the top transistor from switching transients. Because both emitters are at an ac ground point, expensive drive transformers can now be replaced by lower cost capacitively–coupled drive circuits.

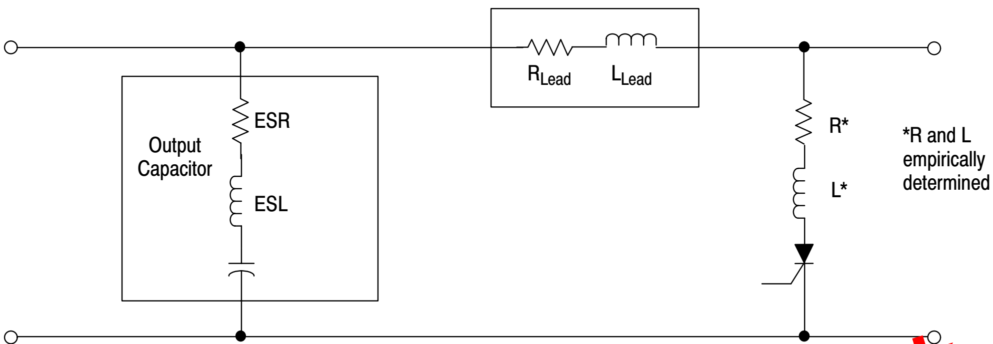
Figure 12–7. Full–Bridge Converter
(200 W to 1.0 kW)



the SCR, as shown in Figure 14–3. Of course, this reduces the circuit's ability to rapidly reduce the dc bus voltage, and a tradeoff must be made between speedy voltage reduction and di/dt.

2. Surge Current — If the peak current and/or the duration of the surge is excessive, immediate destruction due to device overheating will result. The surge capability of the SCR is directly proportional to its die area. If the surge current cannot be reduced (by adding series resistance, see Figure 14–3) to a safe level which is consistent with the system's requirements for speedy bus voltage reduction, the designer must use a higher current SCR. This may result in the average current capability of the SCR exceeding the steady state current requirements imposed by the dc power supply.

Figure 14–3. Circuit Elements Affecting SCR Surge & di/dt



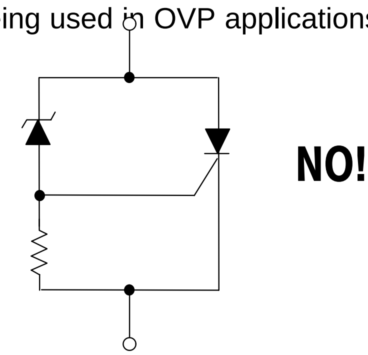
(For additional information on SCRs in crowbar applications refer to *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, ON Semiconductor AN789).

C. The Sense and Drive Circuit

In order to maximize the crowbar SCR's di/dt capability, it should receive a fast rise time high–amplitude gate–drive signal. This must be one of the primary factors considered when selecting the sensing and drive circuitry. Also important is the sense circuitry's noise immunity.

Noise immunity can be a major factor in the selection of the sense circuitry employed. If the sensing circuit has low immunity and is operated in a noisy environment, nuisance tripping of the OVP circuit can occur on short localized noise spikes, which would not normally damage the load. This results in excessive system down time. There are several types of sense circuits presently being used in OVP applications. These can be classified into three types: zener, discrete, and "723."

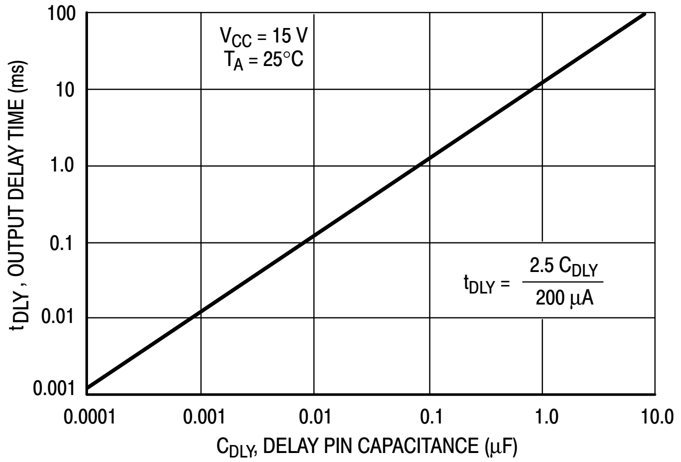
Figure 14–4. The Zener Sense Circuit



1. The Zener Sense Circuit — Figure 14–4 shows the use of a zener to trigger the crowbar SCR. This method is NOT recommended since it provides very poor gate drive and greatly decreases the SCR's di/dt handling capability, especially since the SCR steals its own very necessary gate drive as it turns on. Additionally, this method does not allow the trip point to be adjusted except by zener replacement.

2. The Discrete Sense Circuit — A technique which can provide adequate gate drive and an adjustable, low temperature coefficient trip point is shown in Figure 14–5. While overcoming the disadvantages of the zener sense circuit, this technique requires many components and is more costly. In addition, this method is not particularly noise immune and often suffers from nuisance tripping.

Figure 14–13. Output Delay Time versus Delay Capacitance

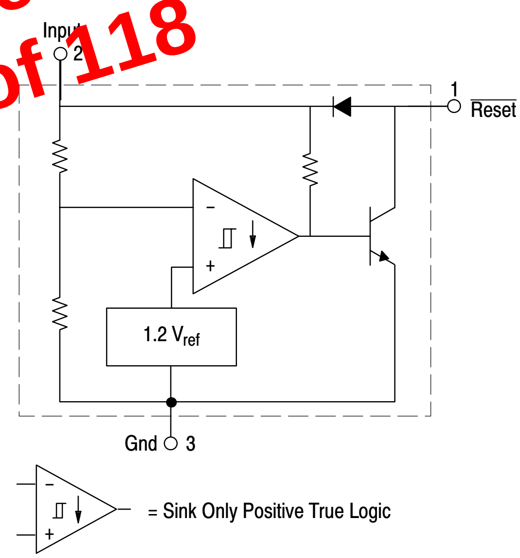


E. MC34064 and MC34164 Series

The MC34064 and MC34164 series are two families of undervoltage sensing circuits specifically designed for use as reset controllers in microprocessor–based systems. They offer the designer an economical solution for low voltage detection with a single external resistor. Both parts feature a trimmed bandgap reference, and a comparator with precise thresholds and built–in hysteresis to prevent erratic reset operation.

The two families of undervoltage sensing circuits, taken together, cover the needs of the most commonly specified power supplies used in MCU/MPU systems. Key parameter specifications of the MC34164 family were chosen to complement the MC34064 series. The table summarizes critical parameters of both families. The MC34064 fulfills the needs of a 5.0 V ± 5% system and features a tighter hysteresis specification. The MC34164 series covers 5.0 V ± 10% and 3.0 V ± 5% power supplies with significantly lower power consumption, making them ideal for applications where extended battery life is required such as consumer products or hand held equipment.

Applications include direct monitoring of the 5.0 V MPU/logic power supply used in appliance, automotive, consumer, and industrial equipment. The MC34164 is specifically designed for battery powered applications where low bias current (1/25th of the MC34064's) is an important characteristic.



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1. *Characterizing the SCR for Crowbar Applications*, Al Pshaenich, ON Semiconductor AN789. **(Out of Print)**
2. *Semiconductor Considerations for DC Power Supply SCR Crowbar Circuits*, Henry Wurzburg, Third National Sold–State Power Conversion Conference, June 25, 1976.
3. *Is a Crowbar Enough?* Willis C. Pierce Jr., Hewlett–Packard, Electronic Design 20, Sept. 27, 1974.
4. *Transient Thermal Response — General Data and Its Use*, Bill Roehr and Brice Shiner, ON Semiconductor AN569. **(Out of Print)**

Heatsink Design Example

Design a flat rectangular heatsink for use with a horizontally mounted power device on a PC board, given the following:

1. Heatsink θ_{SA} = 25°C/W
2. Power to be dissipated, P_D = 2.0 W
3. Maximum ambient temperature, T_A = 50°C
4. Heatsink to be constructed from 1/8″ (0.125″) thick anodized aluminum.
   a) First, a trial heatsink is chosen: 2″ × 3″ (experience will simplify this selection and reduce the number of necessary iterations.)
   b) The factors in Equation (15.3) are evaluated by using the Figures and Tables given:

$$
\begin{aligned}
A &= 2'' \times 3'' = 6 \text{ sq. in.} \\
L &= 6/5'' = 1.2 \text{ in. (from Table 15–3)} \\
T_S - T_A &= 50°\text{C (from Figure 15–4)} \\
h_c &= 5.8 \times 10^{-3} \text{ W/in}^2 - °\text{C (from Figure 15–1)} \\
F_c &= 0.9 \text{ (from Table 15–3)} \\
H_r &= 6.1 \times 10^{-3} \text{ W/in}^2 - °\text{C (from Figure 15–2)} \\
\in &= 0.9 \text{ (from Table 15–4)} \\
h_T &= \text{Fchc} + H_{r\in} = 10.7 \times 10^{-3} \text{ W/in}^2 - °\text{C} \\
\alpha &= 0.13 \text{ (from Figure 15–3)} \\
D &= 1.77 \text{ (from Figure 15–4)} \\
\eta &> 0.94 \simeq 1 \text{ (from Figure 15–3)}
\end{aligned}
$$

   c) Using Equation (15.3), find θ_{SA}:

$$\theta_{SA} \simeq \frac{1}{A\eta(\text{Fchc} + \in H_r)} \simeq 16.66°\text{C/W} < 25°\text{C/W}$$

   d) Since 2″ × 3″ is too large, try 2″ × 2″. Following the same procedure, θ_{SA} is found to be 25°C/W, which exactly meets the design requirements.

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Thermal Information

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}\,(\text{typ})}$$

where:
$P_{D(T_A)}$ = power dissipation allowable at a given operating ambient temperature,
$T_{J(max)}$ = maximum operating junction temperature as listed in the maximum ratings section,
T_A = desired operating ambient temperature,
$R_{\theta JA}$ (typ) = typical thermal resistance junction–to–ambient.

Maximum Ratings

Rating	Symbol	Value	Unit
Operating Ambient Temperature Range	T_A	0 to +70 – 40 to +85	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	– 55 to +150	°C