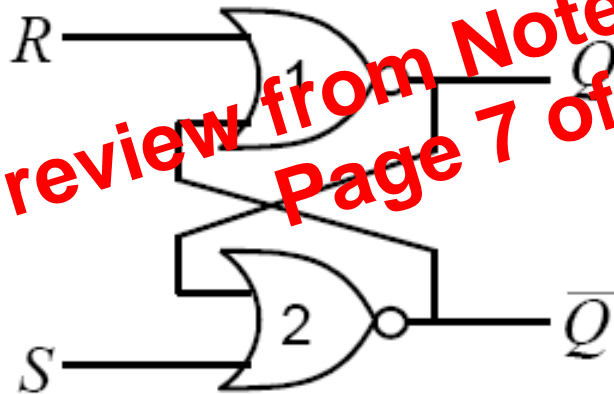


RS Latch - Operation

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NOR truth table

a	b	y
0	0	1
0	1	0
1	0	0
1	1	0

b complemented
always 0

- $S = 1$ and $R = 0$
 - Gate 1 into ‘complement’ condition, $Q = 1$
 - Gate 2 in ‘always 0’ condition, $\bar{Q} = 0$
- This is the (S)et condition

RS Latch - Operation

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NOR truth table

a	b	y
0	0	1
0	1	0
1	0	0
1	1	0

b complemented
always 0

- $S = 1$ and $R = 1$
 - Gate 1 in ‘always 0’ condition, $Q = 0$
 - Gate 2 in ‘always 0’ condition, $\bar{Q} = 0$
- This is the illegal condition

Boolean Algebra

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- **Commutation**

$$a + b = b + a$$

$$a.b = b.a$$

- **Association**

$$(a + b) + c = a + (b + c)$$

$$(a.b).c = a.(b.c)$$

- **Distribution**

$$a.(b + c + \dots) = (a.b) + (a.c) + \dots$$

$$a + (b.c\dots) = (a + b).(a + c)\dots \quad \text{NEW}$$

- **Absorption**

$$a + (a.c) = a \quad \text{NEW}$$

$$a.(a + c) = a \quad \text{NEW}$$

Transparent D Latch

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- We now modify the RS Latch such that its output state is only permitted to change when a valid enable signal (which could be the system clock) is present
- This is achieved by introducing a couple of AND gates in cascade with the R and S inputs that are controlled by an additional input known as the *enable* (EN) input.

Other Types of Flip-Flops

- Consequently we will only consider synchronous circuit design using D-type FFs
- However for completeness we will briefly look at the truth table for J-K and T type FFs

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Timing

- Various timings must be satisfied if a FF is to operate properly:
 - *Setup time*: Is the minimum duration that the data must be stable at the input before the clock edge
 - *Hold time*: Is the minimum duration that the data must remain stable on the FF input after the clock edge

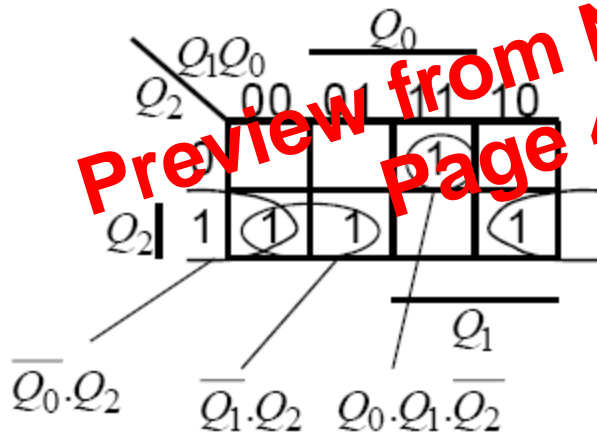
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Characteristic and Excitation Tables

- Characteristic and excitation tables can be determined for other FF types.
- These should be used in the design process if D-type FFs are not used
- We will now determine the modified state transition table for the example 0 to 7 up-counter

Synchronous Counter Example

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So,

$$D_2 = \overline{Q_0} \cdot Q_2 + \overline{Q_1} \cdot Q_2 + Q_0 \cdot Q_1 \cdot \overline{Q_2}$$

$$D_2 = Q_2 \cdot (\overline{Q_0} + \overline{Q_1}) + Q_0 \cdot Q_1 \cdot \overline{Q_2}$$

