Edge-Triggered S-R Flip-flop

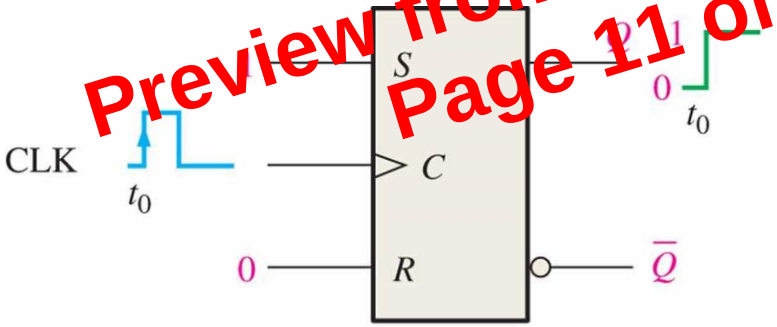
- The **S and R input** of the S-R latch are called **synchronous inputs** as data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse.

INPUTS			OUTPUTS		COMMENTS
S	R	CLK	Q	Q′	
0	0	X	Q_0	Q_0'	No Change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

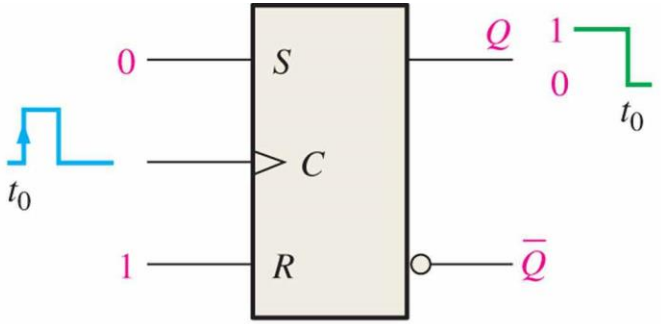
Function table

Edge-Triggered S-R Flip-flop

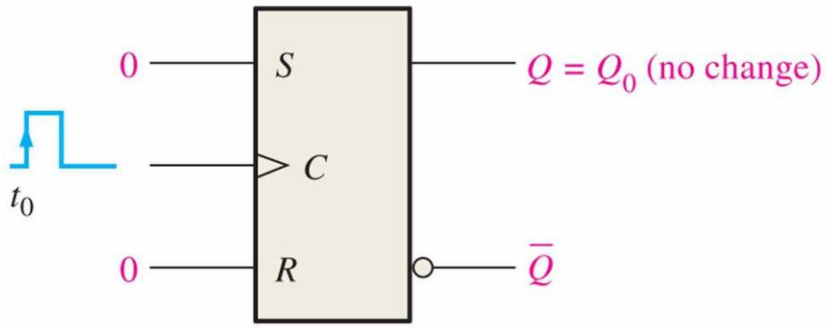
Basic Operation of Positive Edge-Triggered S-R Flip-flop



(a) $S = 1$, $R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $S = 0$, $R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0$, $R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

Edge-Triggered S-R Flip-flop

REMEMBER:

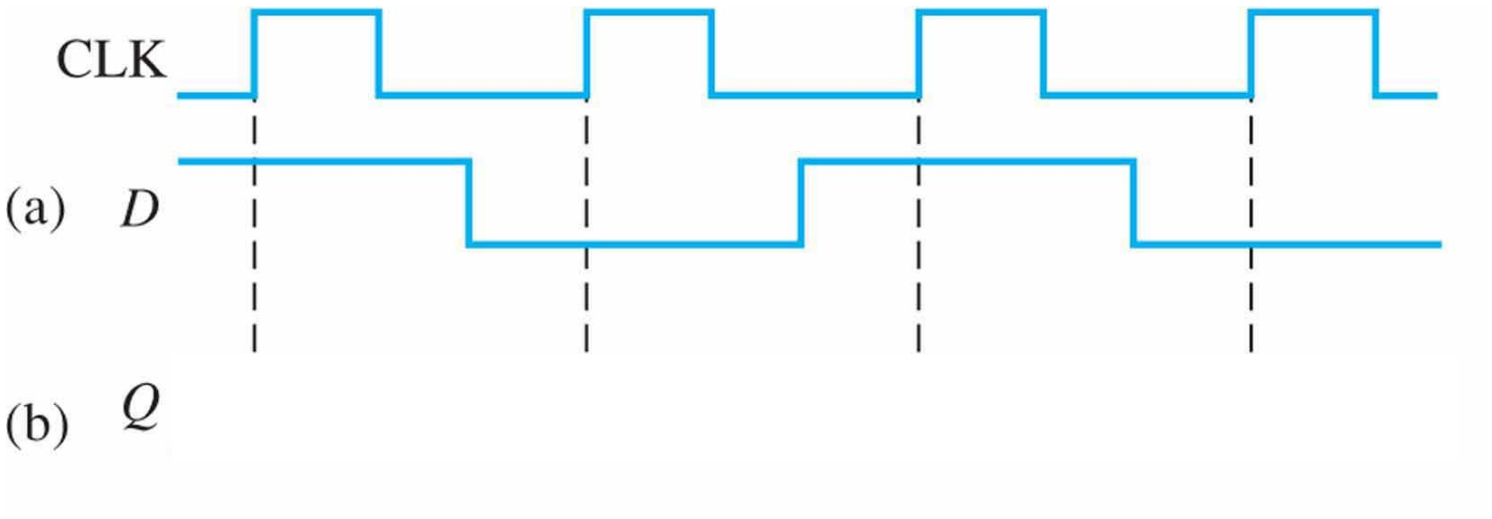
- Flip-flop cannot change state except on the triggering edge of a clock.

- The S-R inputs can be changed at any time when the clock input is LOW or HIGH (*except for a very short interval around the triggering transition of the clock*) without affecting the output.

Edge-Triggered D Flip-flop

- **Example 2**:

Given the waveform for D input and the clock, determine the Q output waveform if the FF start out RESET.



Exercises

- For a positive edge-triggered J-K flip-flop with inputs shown, determine the output. Assume that Q starts low.