A control transfer can have up to three stages. The Setup Stage is where the request is sent. This consists of three packets. The setup token is sent first which contains the address and endpoint number. The data packet is sent next and always has a PID type of data0 and includes a setup packet which details the type of request. The last packet is a handshake used for acknowledging successful receipt or to indicate an error. If the function successfully receives the setup data (CRC and PID etc OK) it responds with ACK, otherwise it ignores the data and doesn't send a handshake packet. Functions cannot issue a STALL or NAK packet in response to a setup packet.

D. Transaction transfer

In all 4 different transfers of Control, Bulk, Interrupt and Isochronous, these 4 transfers consist of 3 types of packets namely the

1- Token packet

It consists of the following elements: sync sequence, Package identifier, device address, endpoint number and 5-bit Cyclic Redundancy Check (CRC). Tokens are only sent by the host, not by a device.

2- Data transfer packet

It consists of the following elements: sync sequence, package identifier, data and 16-bit Cyclic Redundancy Check (CRC). Also, the data must be sent in multiples of bytes.

3- Handshake.

They are generally sent in response to data packets. It consists of the following elements: sync sequence and Package identifier.

Fig.7 NRZI transmission scheme

E. Conclusion

I^2C bus is used by many integrated circuits and is simple to implement. Microcontrollers can communicate with I^2C devices even if it has no special I^2C interface.I^2C bus can communicate with slow devices and can also use high speed modes to transfer large amounts of data.

The SPI bus is a simple 4 wired bus. It is easy to be configured. It can be connected to many devices (slaves), but as the number of slaves increases the number of wires will increase which will increase the area of the circuit, so this is an undesired property.

USB3 is fast and complicated serial Bus, it has a very big bandwidth (up to 5Gbps) , low power consumption, increased power output and compatible with USB2, for that it is the most common usable port in computers, mobiles and a lot of applications.S

REFERENCES

[1] Bollam Eswari, N.Ponmagal, K.Preethi, S.G.Sreejeesh "Implementation of I2C Master Bus Controller on FPGA" IEEE's paper, April 2013.
Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp&arnumber=6577229&sortType%3Ddesc_p_Publication_Year%26searchField%3DSearch_All%26queryText%3Di2c

[2] Peter Corcoran "Two Wires and 30 Years: A tribute and introductory tutorial to the I²C two-wire bus" IEEE's paper, July 2013.
Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp&arnumber=6556004&sortType%3Ddesc_p_Publication_Year%26searchField%3DSearch_All%26queryText%3Di2c+bus

[3] Shumit Saha, Md. Ashikur Rahman, Amit Thakur "Design and implementation of SPI bus protocol with Built-in-self-test capability over FPGA" IEEE's paper, April 2014.
Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp&arnumber=6919076&queryText%3Dspi+protocol

[4] "USB 3.0 Bus"
Available: http://en.wikipedia.org/wiki/USB_3.0

[5] "I2C Bus"
Available: http://en.wikipedia.org/wiki/I%C2%B2C

[6] "SPI Bus"
Available: http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus