Q. $x = 1000111\underline{000}$

2's complement of x = $0111001\underline{000}$

Q. $x = 1011$

2's of x = 0101

Q. $11010_2 - 01110_2$ = $11010 + (-01110)$

(i). $11010 + (\text{1's of } 01110)$ = $11010 + 10001$

EOC ① 01011

$+1$

01100

(ii). $11010 + (\text{2's of } 01110)$

$= 11010 + 10010$

EOC ignore ① 01100

Q. $01110_2 - 11010_2$ = $01110 + (\text{2's of } 11010)$

$= 01110 + 00110$

NO EOC $\rightarrow$ □ 10100

$\downarrow$ 2's

Negative sign -01100

$2^4 = 16$

$16 - 2 = 14$

$16 - 1 = 15$

1's comp	2's comp
$+0 = 0000$	$+0 = 0000$
-0 = 1's comp of $+0$	-0 = 2's comp. of $+0$
= 1's of 0000	= 0000
= 1111 ← (Disadv. of 1's complement)	

* Range of numbers represented using 'n' bits

Go represent (16) numbers

1's comp. form $\longrightarrow$ $+(2^{n-1}-1)$ to $-(2^{n-1}-1)$

let $n=4$ $\Rightarrow$ $+7$ to -7 $\longrightarrow$ (14)

2's comp. form $\Rightarrow$ $+(2^{n-1}-1)$ to -2^{n-1}

let $n=4$ $\Rightarrow$ $+7$ to -8 $\longrightarrow$ (15)

Q. How many bits are required to represent -64_{10} in a). 1's comp. form b). 2's form

1's form $\Rightarrow$ $+(2^{n-1}-1)$ to $-(2^{n-1}-1)$

let $n=7$ $\rightarrow$ $+63$ to -63

✓ $n=8$ $\rightarrow$ $+127$ to -127

2's form $\rightarrow$ $+(2^{n-1}-1)$ to -2^{n-1}

✓ let $n=7$ $\Rightarrow$ $+63$ to -64

Q. 10's comp for $(731)_{11}$

$$\begin{array}{rccc} & A & A & A \\ & 7 & 3 & 1 \\ (-) & & & \\ \hline & 3 & 7 & 9 \end{array}$$

Q. 9's comp of $(731)_{10}$

$$\begin{array}{rc} & 999 \\ (-) & 731 \\ \hline & 268 \end{array}$$

Binary Numbers :

(a). Unsigned Numbers $\longrightarrow$

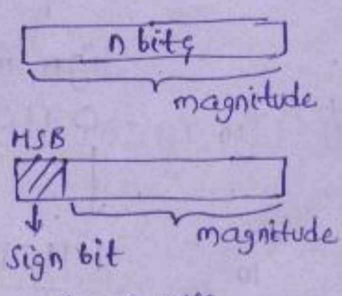
(b). Signed Numbers $\longrightarrow$

$\downarrow$ represented by

(i). sign magnitude

(ii). 1's comp form

(iii). 2's comp form



$0 \rightarrow +ve$

$1 \rightarrow -ve$

These three representations are same for unsigned (+ve Numbers).

minterms & maxterms :

Let $f(A,B,C)$. contains all variables

minterms		maxterms
$\bar{A}\cdot\bar{B}\cdot\bar{C}$		$\bar{A}+\bar{B}+\bar{C}$
$\bar{A}\cdot\bar{B}\cdot C$		$\bar{A}+\bar{B}+C$
8 $\bar{A}\cdot B\cdot\bar{C}$	8	$\bar{A}+B+\bar{C}$
$\vdots$		$\vdots$
$AB\cdot\bar{C}$		$A+B+\bar{C}$
ABC		$A+B+C$

* for 'n' var. function $\rightarrow$ 2^n minterms
  2^n maxterms

* Sum of all minterms = 1. $\sum_{i=0}^{2^n-1} m_i = 1$

* product of all max-terms = 0. $\prod_{i=0}^{2^n-1} M_i = 0$

* product of any two minterms = 0

  $m_i \cdot m_j = 0$, if $i \neq j$
  $= m_i$, if $i = j$

* Sum of any two maxterms = 1.

  $M_i + M_j = 1$, if $i \neq j$
  $= M_i$, if $i = j$.

Let $f(x,y)$

minterm: $1 = var$, $0 = \overline{var}$; maxterm: $1 = \overline{var}$, $0 = var$

x	y	minterm		max term	
0	0	$\bar{x}\cdot\bar{y}$	m_0	$x+y$	M_0
0	1	$\bar{x}\cdot y$	m_1	$x+\bar{y}$	M_1
1	0	$x\cdot\bar{y}$	m_2	$\bar{x}+y$	M_2
1	1	xy	m_3	$\bar{x}+\bar{y}$	M_3

$f = \Sigma m(2, 4)$

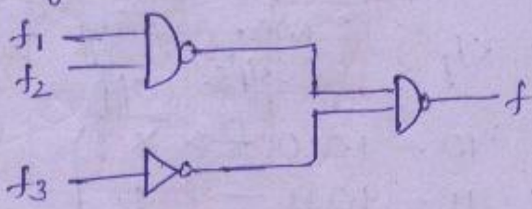
Similarly $f_3 = f_1 - f_2 \Rightarrow f_3 = ?$

$f_3 = \Sigma m(0, 7)$.

$f_4 = f_2 - f_1 \Rightarrow f_4 = ?$

$f_4 = \Sigma m(1, 6)$.

Q. Determine the function f_3 in the following logic ckt.



where $f = \Sigma m(0,1,3,5)$

$f_1 = \Sigma m(2,3,6,7)$

$f_2 = \Sigma m(0,1,5)$.

$f = \overline{\overline{f_1 f_2} \cdot \overline{f_3}}$

$= f_1 f_2 + f_3$

$\Rightarrow f_3 = f - f_1 f_2$

But $f_1 \cdot f_2 = \phi$

$\Rightarrow f_3 = f = \Sigma m(0,1,3,5)$.

Q. $f = f_1 \cdot f_2$ where $f_1 = \Sigma m(0,1,5) + d(2,3,7)$

$f_2 = \Sigma m(1,2,4,5) + d(0,7)$.

$f = f_1 \cdot f_2 = \Sigma m(1,5) + d(0,2,7)$.

minterm in one fun. / dont care in another fun.

$1 \cdot d = d$

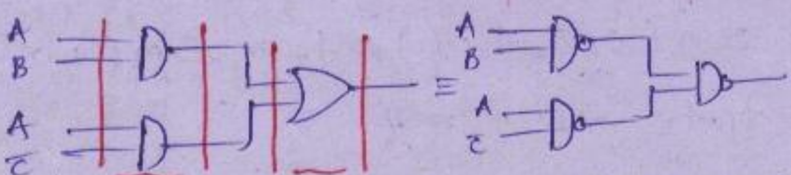
$0 \cdot d = 0$

$1 + d = 1$

$0 + d = d$

Two level logic :-

SOP form $\longrightarrow$ $Y = AB + A\bar{C}$

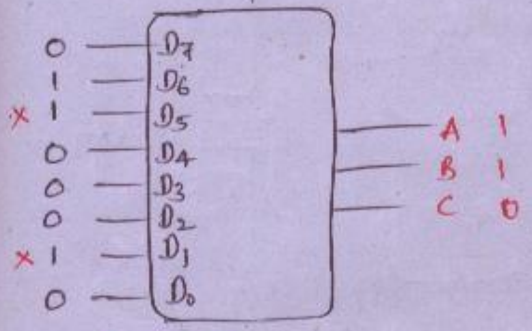


AND - OR logic $\equiv$ NAND - NAND

PRIORITY ENCODER: (74 LS 148)

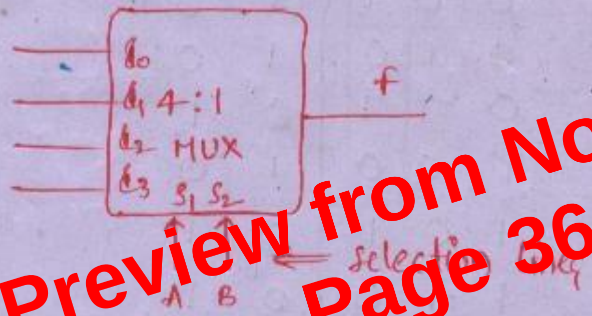
D_7 – highest priority

D_0 – lowest priority



x – ignored

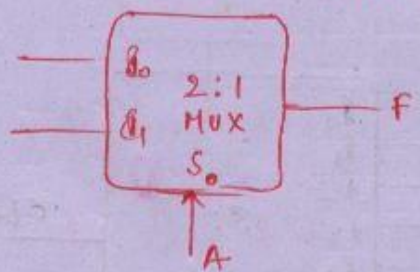
MULTIPLEXER:



A	B	f
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

for 4:1 MUX,

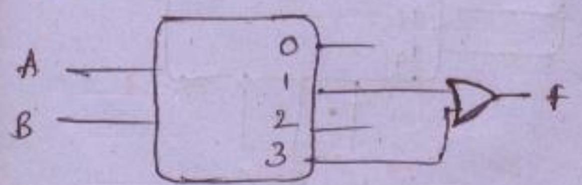
$$f = \bar{A}\bar{B} I_0 + \bar{A} B I_1 + A \bar{B} I_2 + A B I_3$$
$$= m_0 I_0 + m_1 I_1 + m_2 I_2 + m_3 I_3 .$$



for 2:1 MUX,

$$f = \bar{A} I_0 + A I_1$$

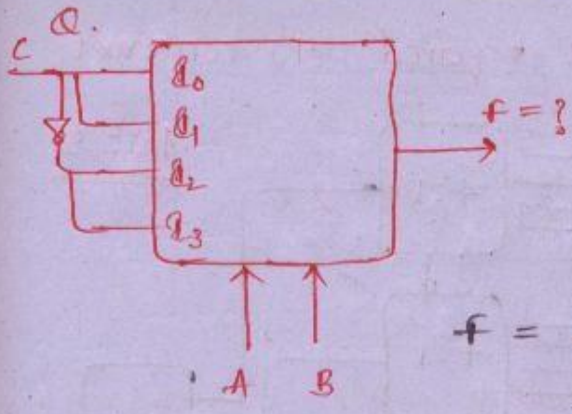
Q.



$f(A,B) = \Sigma m(1,3)$

decoder

Q.



Given that

$I_0 = I_1 = C$

$I_2 = I_3 = \overline{C}$.

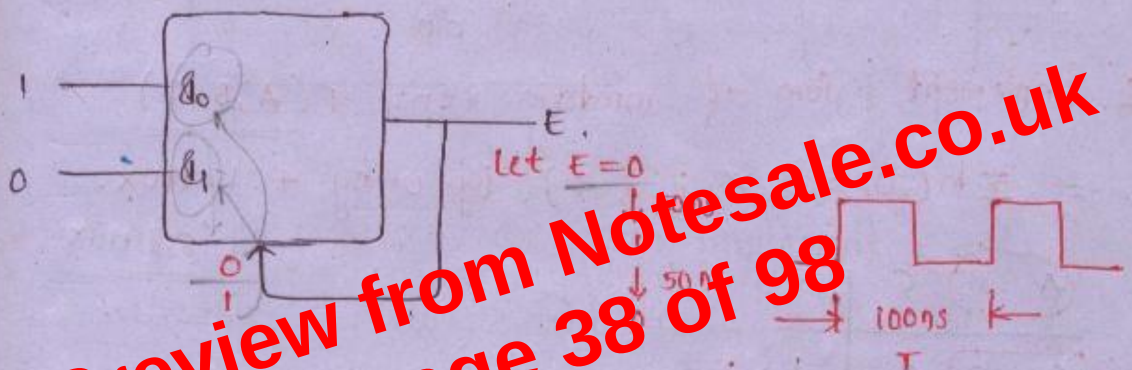
$$f = \overline{A}\,\overline{B}C + \overline{A}BC + A\overline{B}\,\overline{C} + AB\overline{C}$$

$$= \overline{A}C(\overline{B}+B) + A\overline{C}(\overline{B}+B)$$

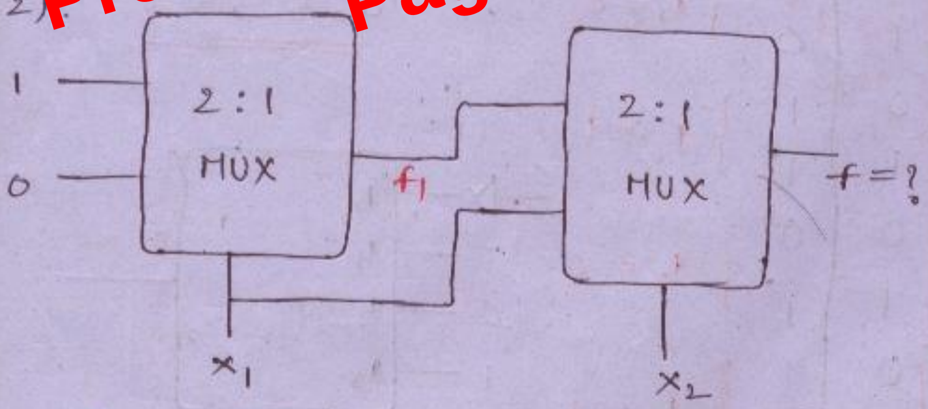
$$= A \oplus C.$$

Q. Determine the o/p's of the following MUX's?

1). Switching speed is 50 ns.



2)



$f_1 = \overline{A}I_0 + AI_1$

$f_1 = \overline{x_1}\cdot 1 + x_1\cdot 0 = \overline{x_1}$

$f = \overline{A}I_0 + AI_1$

$= \overline{x_2}\cdot\overline{x_1} + x_2\cdot x_1$

$= x_2 \odot x_1$

CHAR. TABLE :

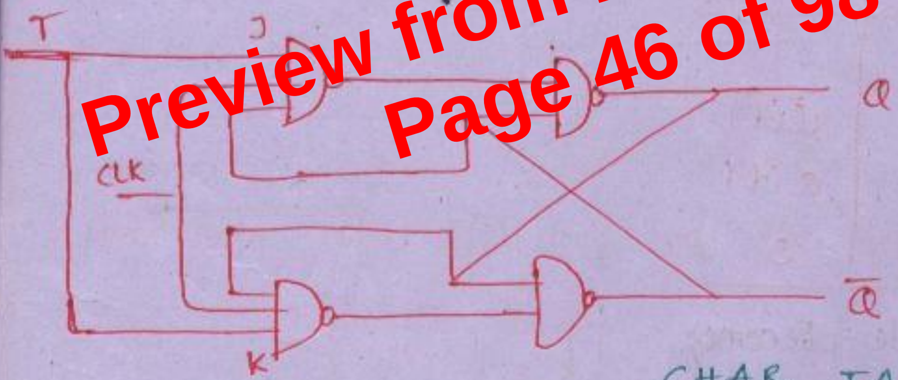
J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

J \ KQ	00	01	11	10
0	0	1	0	0
1	1	1	0	1

$Q(t+1) = J\bar{Q} + \bar{K}Q$

CLOCKED T- FLIP FLOP :

T - TOGGLE



TRUTH TABLE :-

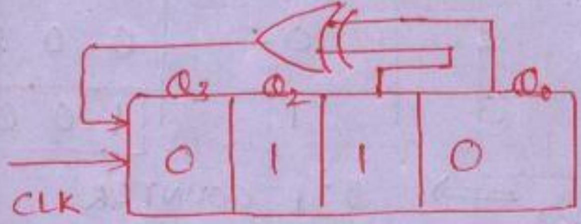
	T	Q(t+1)
J=K=0 ←	0	Q(t)
J=K=1 ←	1	$\overline{Q(t)}$

CHAR. TABLE :-

T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

$\therefore Q(t+1) = T \oplus Q$

Q. In the following shift reg. how many CP's are required to make shift reg. content to have all one's.



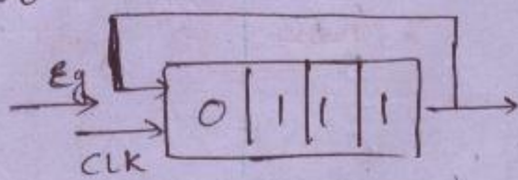
CLK	Serial i/p ($Q_1 \oplus Q_0$)	Q_3	Q_2	Q_1	Q_0
0	—	0	1	1	0
1	1	1	0	1	1
2	0	0	1	0	1
3	1	1	0	1	[illegible]
4	1	[illegible]	1	0	1
5	[illegible]	[illegible]	1	1	0
6	1	1	1	1	1

APPLICATIONS OF SHIFT REG'S:

(1). Serial to parallel & parallel to serial convertion

(2). Time delays - SISO

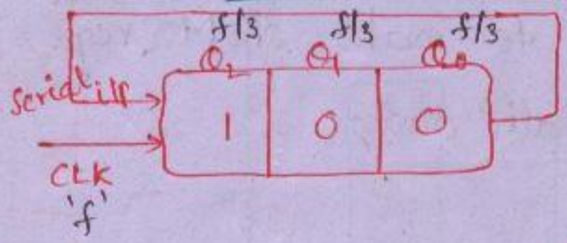
(3). Sequence Generator



(4). Counter → RING
→ JOHNSON.

.... 0111011101110111.

RING COUNTER:

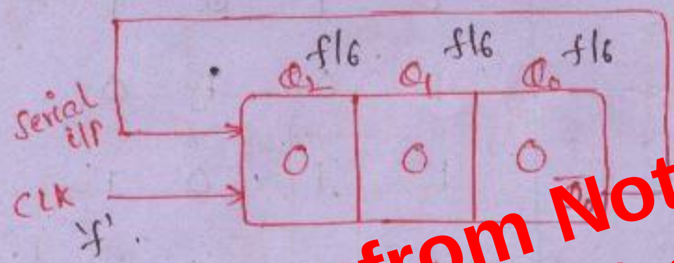


CLK	Serial i/p (Q_0)	Q_2 Q_1 Q_0
0	—	$\boxed{1\ 0\ 0}$
1	0	0 1 0
2	0	0 0 1
3	1	$\boxed{1\ 0\ 0}$

$\Longrightarrow$ 3:1 COUNTER

N - bit Ring Counter:
→ counting capacity = N:1
→ output frequency = f/N.

JOHNSON COUNTER: [TWISTED RING COUNTER].



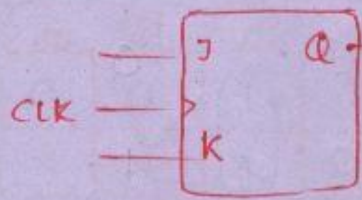
CLK	Serial i/p ($\bar{Q_0}$)	Q_2	Q_1	Q_0
0	—	0	0	0
1	1	1	0	0
2	1	1	1	0
3	1	1	1	1
4	0	0	1	1
5	0	0	0	1
6	0	0	0	0

$\Longrightarrow$ 6:1 COUNTER.

N - Bit Johnson Counter:
→ Counting capacity = 2N:1
→ Output frequency = f/2N.

Excitation Tables :

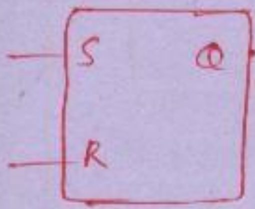
J	K	Q(t+1)
~~0~~	~~0~~	Q(t)
~~0~~	~~1~~	0
1	0	1
1	1	$\overline{Q(t)}$



Q(t)=0
Q(t+1)=1

J	K
1	0
1	1
1	x .

SR f/f :



Q(t) = 0
Q(t+1) = 0

S	R
0	1
0	0
0	[illegible]

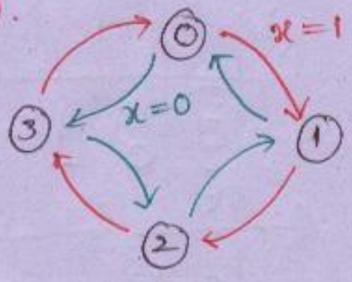
Q(t)	Q(t+1)	J	K	S	R		D
0	0	0	x	0	x	0	0
0	1	1	x	1	0	1	1
1	0	x	1	0	1	1	0
1	1	x	0	x	0	0	1

Q. Obtain Excitation table of x-y f/f :-

x	y	Q(t+1)
0	0	1
0	1	$\overline{Q(t)}$
1	0	Q(t)
1	1	0

Q. Draw the state diagram of following digital circuit (i.e. 2 bit syn. up/down counter).

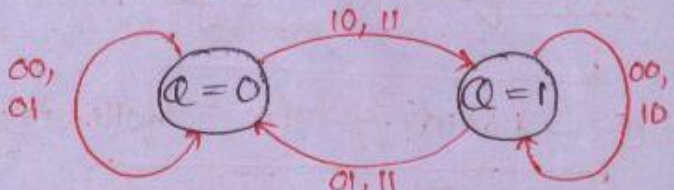
(i).



(ii). JK - f/f

present i/p's { J, k $\longrightarrow$ branches of each state.

P.S { Q $\longrightarrow$ states

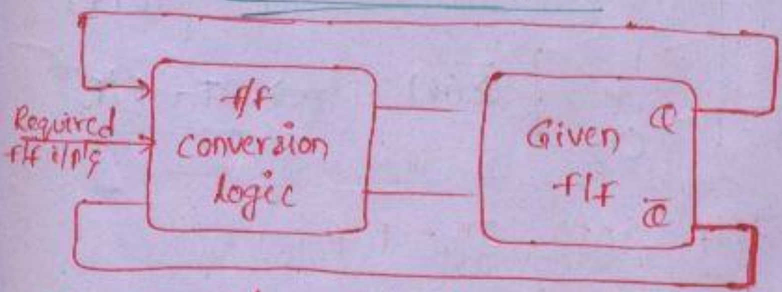


(iii). T- f/f

- T $\longrightarrow$ present i/p
- Q $\longrightarrow$ P.S.

T	Q (t+1)
0	Q (t)
1	$\bar{Q}$ (t)

CONVERSION OF f/f's :



Q. Convert SR-f/f into T-f/f.

SR f/f $\longrightarrow$ T-f/f

exci. table   char. table

T	Q (t)	Q(t+1)	S	R
0	0	0	0	×
0	1	1	×	0
1	0	1	1	0
1	1	0	0	1

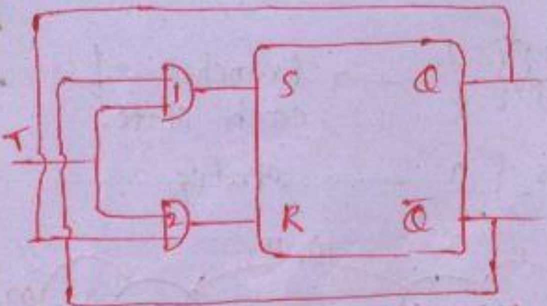
T \ Q	0	1
0	0	X
1	1	0

$S = T\bar{Q}$

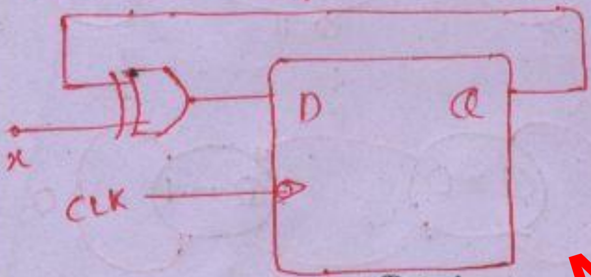
T \ Q	0	1
0	X	0
1	0	1

$R = TQ$

→ T-f/f



Q. Identify the following f/f.



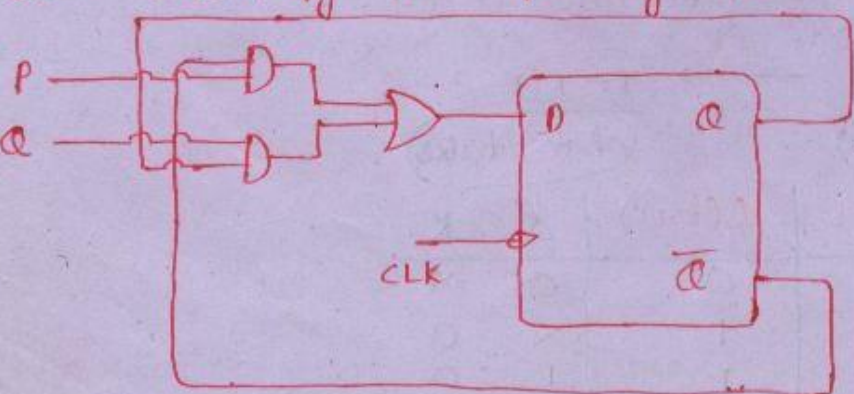
x	Q(t)	$x \oplus Q$	Q(t+1)	
0	0	0	0	Q(t)
0	1	1	1	
1	0	1	1	$\overline{Q(t)}$
1	1	0	0	

x	Q(t+1)
0	Q(t)
1	$\overline{Q(t)}$

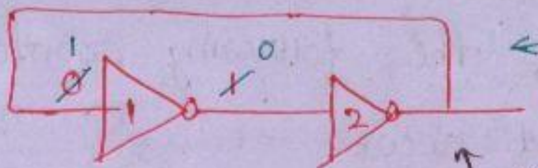
⟹ T-f/f

Q. Convert D-f/f into JK-f/f.

Q2. Identify the following f/f.



* MON 08/12/08 *

(1). 

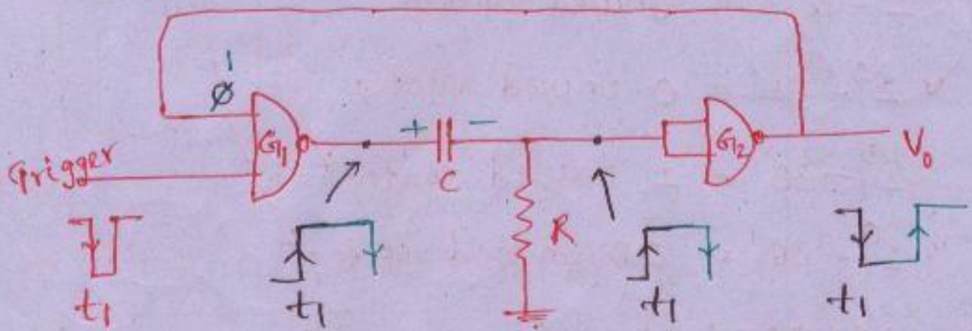
← BISTABLE MV

$V_0 = \cancel{0}\ 1$

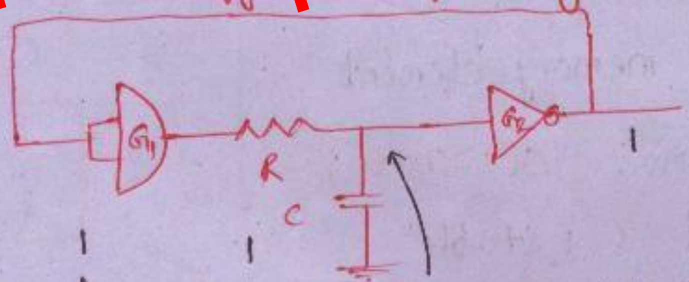
↑ Even no. of inverters

(2). flip flop

MONO STABLE :



Q. Identify the following MV's.



1 ↓ 0   1 ↓ 0   no voltage = '0' logic

1 ← charged   0

⟶ NO trigger ; Ans: ASTABLE MV.

EPROM | RAM

$\boxed{27}16 = 2\text{ kB} \leftarrow \boxed{61}16$

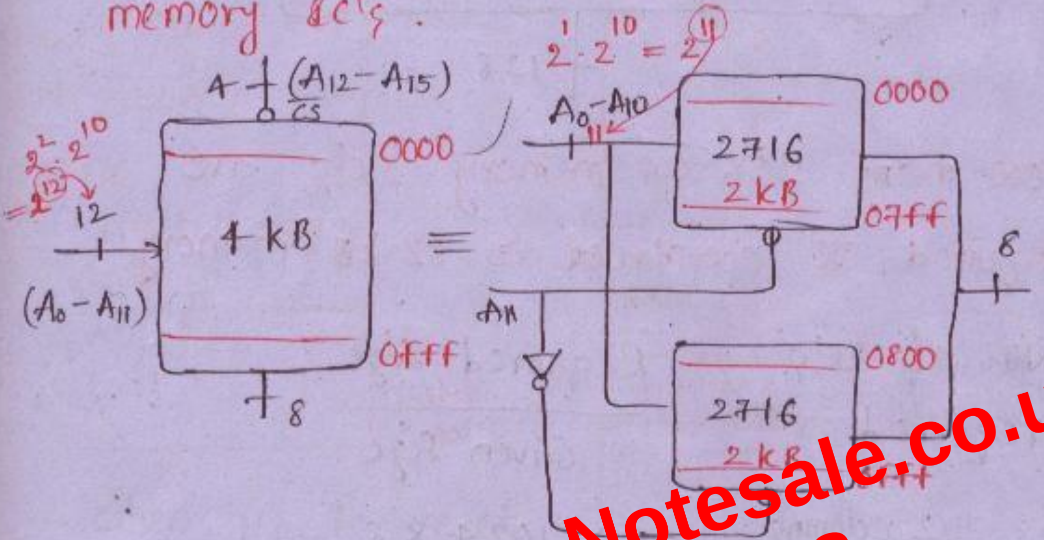
$27\frac{16}{8} = 2\text{ kB} \leftarrow 6116$

$27\frac{32}{8} = 4\text{ kB} \leftarrow 6132$

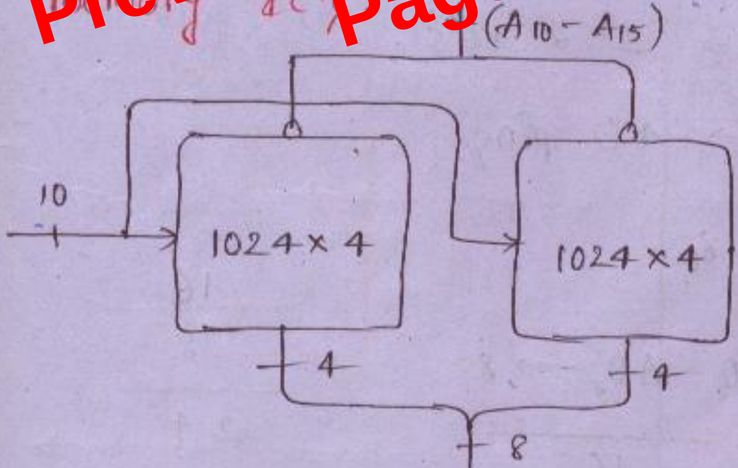
$27\frac{64}{8} = 8\text{ kB} \leftarrow 6164$

$27\frac{128}{8} = 16\text{ kB} \leftarrow 61128$

Q. Construct a 4 kB memory using 2716 memory IC's.



Q. construct a 1kB memory using 1024×4 memory IC's



$\frac{1\text{kB}}{1024 \times 8}$

Q. The add. lines of 64 memory IC having capacity of 256×2 are connected together. what is the size of resulting memory

Instruction	Operation	Bytes/M/C/T	Types of M/C	flags affected.
1). ADD R (R → B, C, D, E, H, L, A.)	$A + R \rightarrow A$	1/1/4	F	ALL
ADD M	$A + (HL) \rightarrow A$	1/2/7	F, R	ALL
ADI 8bit data	$A + (8bit\ data) \rightarrow A$	2/2/7	F, R	ALL
2). SUB R				
SUB M				
SUI 8bit data				
3). ADC R	$Cy + A + R \rightarrow A$	1/1/4		
ADC M	$Cy + A + (HL) \rightarrow A$	1/2/7		
ACI 8bit data	$Cy + A + (8bit\ data) \rightarrow A$	2/2/7		
4). SBB R				
SBB M	$A - (HL) - Cy \rightarrow A$	1/2/7		
SBI 8bit data				

5).	INR R	R+1 → R	1/1/4	F	ALL except 'cy' flag
	DCR R	R−1 → R	1/1/4	F	
	INR M	(HL)+1 → (HL)	1/2/10	F, R, W	ALL except 'cy' flag
	DCR M	(HL)−1 → (HL)	1/2/10	F, R, W	
	INX rp	rp+1 → rp	1/1/6	S	NO FLAGS
	DCX rp	rp−1 → rp	1/1/6	S	

S = opcode fetch m/c (6T)

B = Bus idle m/c (3T)

BC = 8250,

INR B — B = 83

INX B — BC = 8251.

6).	DAD rp	HL+rp → HL	1/3/10	F, B, B	Only 'cy' flag.

LOGICAL INSTRUCTIONS:

1).	ORA R	$A \vee R \rightarrow A$	ALL but $C_y = 0$.
	ORA M	$A \vee (HL) \rightarrow A$	
	ORI 8bitdata	$A \vee$ 8bitdata $\rightarrow A$	