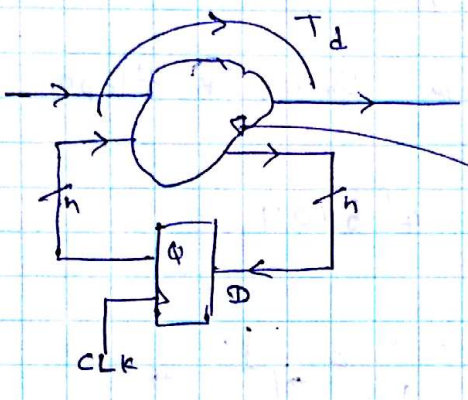
defined for the flop

- Set up time & hold time depend on the physical characteristics of the transistors. - Slide 32
- This check has to be done for each & every flop in the ckt. (Timing Analysis) ↗
  3 states → How many flops → 2 (1 flop can have 2)

01/01/2017



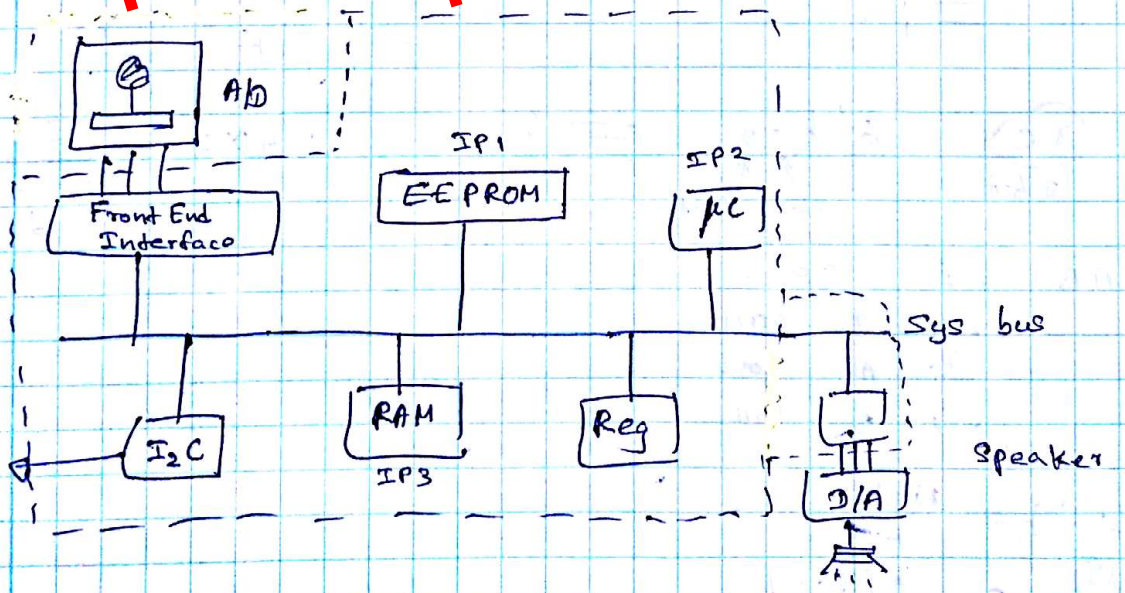
CLK - 1 ns

Delay in this combinational ckt (propagation delay) should be less than 1 ns.

- We first choose the ckt frequency & then select the component according to that.
- Transister size ↑ → propagation delay ↑ (due to capacitance)

RTL Coding & Verification

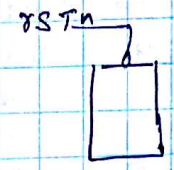
Voice recorder.



- Hard IP :- Everything is done. Can copy & paste.
- Soft IP :- Only the code.

```
input  CLK, RSTn
input  [3:0] D;
reg
```

```
always @ (posedge clk or negedge rstn )
    if ( ! RST )
        q <= 4'b0;
    else
        q <= D;
```



Slide 33.

Initial block is not used in RTL. Only in verification.

```
repeat ( 5 )
    x = x + 1;
```

⇒ "unlooped as this"

```
x = x + 1
x = x + 1      5 times
  :
x = x + 1
```

Slide 34

✗ If Else have a priority ~~of~~ for if. If "if" is selected "else" part is neglected.

Case

$display, monitor commands not belong to RTL. Those are for verification.

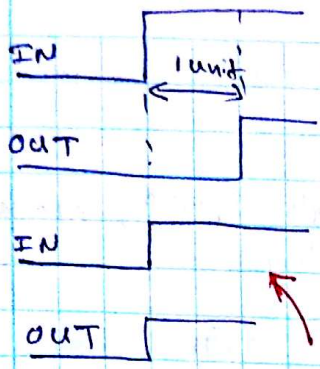
✗ Task → sequential cct. take many clock cycles

✗ Function → Combinational cct. Can have many combinational ccts inside a one function.

Timing Constant.

```
a <= #1 b;    { a is assigned b after 1 time unit delay }
```

used in simulation to get correct results.



⇒ out = #1 In ;

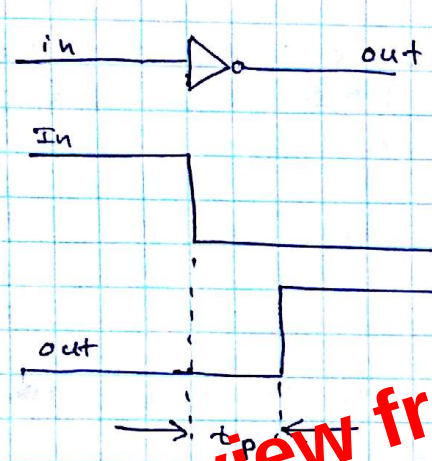
{out will change after 1' time delay when In changes}

⇒ OUT = IN ;

This is ~~exhaust~~ real implementation. But in real hardware there are some propagation delays. So this never happens.

~~When~~ In the real implementation there may be delays due to propagation. So to represent those we use #u time delays.

① Delay Specification



more disterbence to current carrying electrons

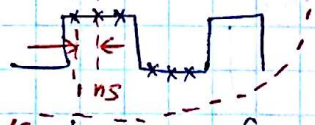
× ↑ Temp ∝ Delay ↑ t_p

× ↑ Voltage ⇒ Delay ↓ t_p

× foundary process ⇒ Delay

× When powering up we reset the flipflops. (To control internal inputs).

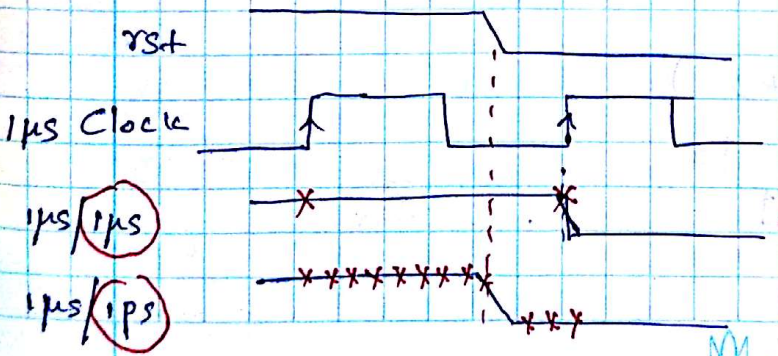
eg:- Time scale = 10 ns / 1 ns Precision.

clock → 

1 MHz → 1 µs

a ⇐ #1 5 ; (after 10 nano seconds, a ⇐ 5).

In every nano second we calculate values.



← can't detect the accurate value change position due to low precision.