Verilog Sample Problem

Create a Verilog description of a 4-input function that outputs a ‘1’ if the number of 1’s at the inputs are more than the number of 0’s; otherwise the output is ‘0’. The inputs are A, B, C and D. The output is F.

Truth Table:

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Equation:

F = ABD + ABC + ACD + BCD

F = AB (D + C) + CD (A + B)

Circuit: