INTRODUCTION

- Design problem normally starts with a word description of input output relation and ends with a circuit diagram having sequential and combinatorial logic elements.
- Sequential logic circuit design refers to synchronous clock-triggered circuit because of its design and implementation advantages.
- Design a digital circuit whose outputs are to take on specific values after a specific sequence of inputs has taken place.

State machine design

MOORE MODE	MEALY MODEL
The output depends only on present state and not on input	The output is derived from present state as well as input
It requires more number of states and thereby more hardware to solve any problem	It requires less number of states and thereby less hardware to solve any problem
The output is generated one clock cycle after.	The output is generated one clock cycle earlier, so faster
The output remains stable over entire clock period and changes only when there occurs a state change at clock trigger based on input available at that time.	The glitches occurs

SEQUENCE RECOGNIZER

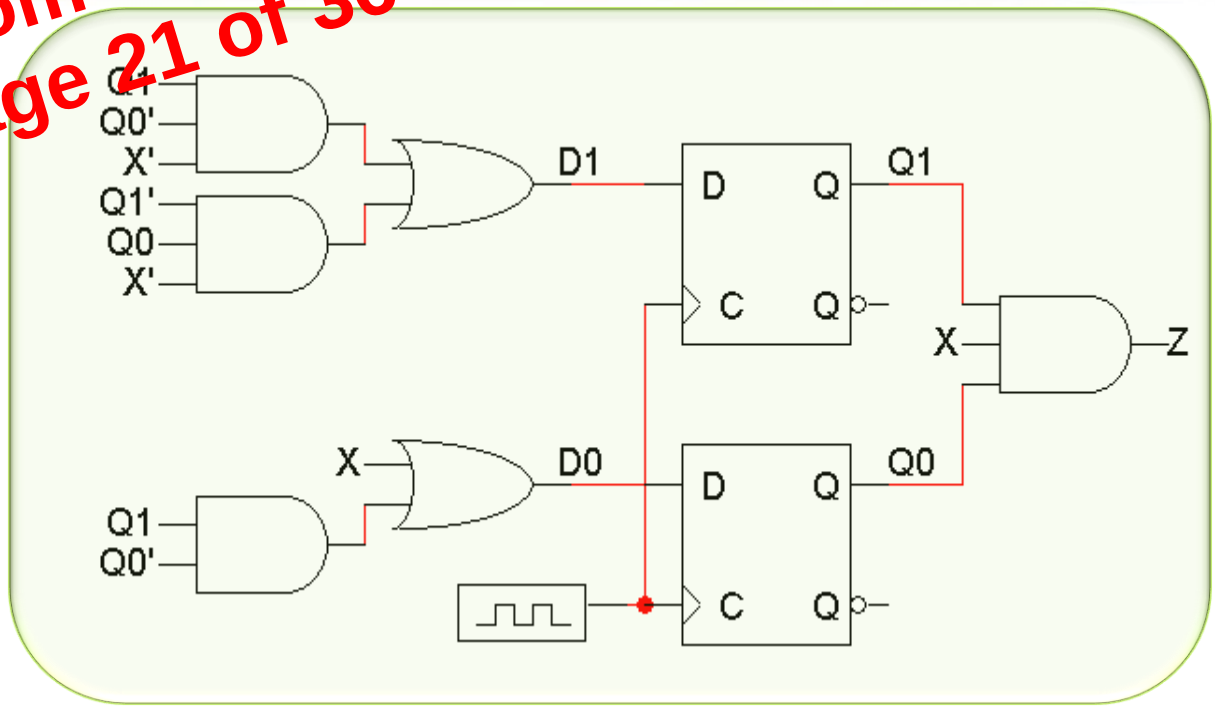
Step: 5 Build the circuit

For Output Z

K-map

X \ Q_1Q_0	00	01	11	10
0	0	0	0	0
1	0	0	1	0

$Z = XQ_1Q_0$



$D_1 = Q_1\ Q_0'\ X' + Q_1'\ Q_0\ X'$

$D_0 = X + Q_1\ Q_0'$

SEQUENCE RECOGNIZER

Step: 2 Assigning binary codes to States

Present	Next		Output	
	X=0	X=1	X=0	X=1
A	B	A	0	0
B	B	C	0	0
C	B	A	1	0

Next State Table

Put A=00
B=01
C=10

Present		Next			
		X=0		X=1	
Q_1	Q_0	Q_1	Q_0	Q_1	Q_0
0	0	0	1	0	0
0	1	0	1	1	0
1	0	0	1	0	0

SEQUENCE RECOGNIZER

Step: 4 Find equations for the FF inputs and output

X=0			X=1		
QP_0	QN_0	T_0	QP_0	QN_0	T_0
0	1	1	0	0	0
1	1	0	1	0	1
0	1	1	0	0	0

K-map for T_0

Q_1Q_0 / x	00	01	11	10
0	1	0	x	1
1	0	1	X	0

$T_0 = X'Q_0' + XQ_0$

SEQUENCE RECOGNIZER

Step: 4 Find equations for the FF inputs and output

X=0			X=1		
QP_0	QN_0	T_0	QP_0	QN_0	T_0
0	0	0	0	1	1
1	0	1	1	1	0
0	0	0	0	1	1

K-map for T_0

x \ Q_1Q_0	00	01	11	10
0	0	1	x	0
1	1	0	X	1

$T_0=X'Q_0+XQ'_0$