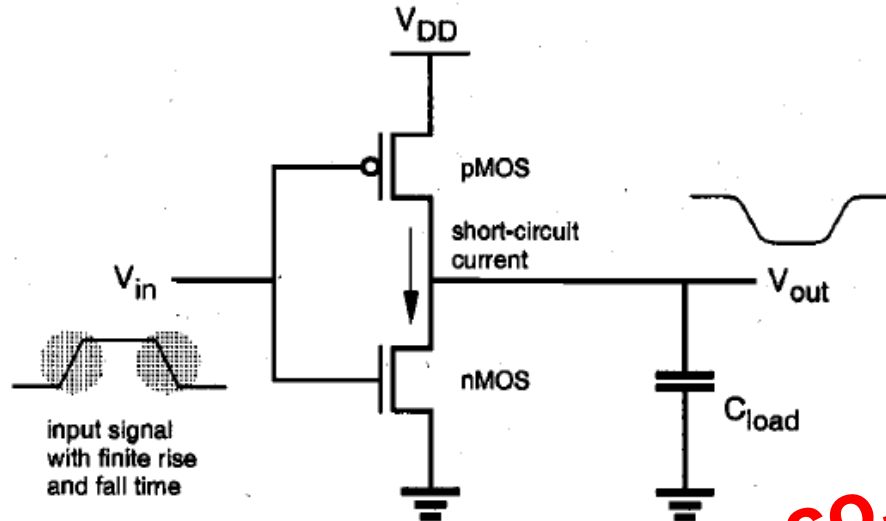


(2) Short-Circuit Power Dissipation:

The switching power dissipation discussed above is purely due to the energy required to charge up the parasitic capacitances in the circuit, and the switching power is independent of the rise and fall times of the input signals. Now, if a CMOS inverter (or a logic gate) is driven with input voltage waveforms with finite rise and fall times, both the nMOS and the pMOS transistors in the circuit may conduct simultaneously for a short amount of time during switching, forming a direct current path between the power supply and the ground, as shown in below Fig.



Both nMOS and pMOS transistor may conduct (simultaneously) a short-circuit current during switching.

Short-circuit current component is the current component which passes through both the nMOS and the pMOS devices during switching. It does not contribute to the charging of the capacitances in the circuit.

This component is particularly powerful if the output load capacitance is small, and/or if the input signals rise and fall times are large, as shown in below Fig. Here, the input/output voltage waveforms and the components of the current drawn from the power supply are illustrated for a symmetrical CMOS inverter with small capacitive load. The nMOS transistor in the circuit starts conducting when the rising input voltage exceeds the threshold voltage $V_{T,n}$.

The pMOS transistor remains on until the input reaches the voltage level $(V_{DD} - |V_{T,p}|)$. Thus, there is a time window during which both transistors are turned on. As the output capacitance is discharged through the nMOS transistor, the output voltage starts to fall. The drain-to-source voltage drop of the pMOS transistor becomes nonzero, which allows the pMOS transistor to conduct as well. The short circuit current is terminated when the input voltage transition is completed and the pMOS transistor is turned off. A similar event is responsible for the short-circuit current component during the falling input transition, when the output voltage starts rising while both transistors are on.

Note the magnitude of the short-circuit current component will be approximately the same during both the rising-input transition and the falling-input transition, assuming that the inverter is symmetrical and the input rise and fall times are identical. The pMOS transistor also conducts the current which is needed to charge up the small output load capacitance, but only during the falling-input transition (the output capacitance is discharged through the nMOS device during the rising-input transition). This current component, which is responsible for the switching power

dissipation of the circuit (current component to charge up the load capacitance), is also shown in Fig. The average of both of these current components determines the total amount of power drawn from the supply.

For a simple analysis consider a symmetric CMOS inverter with $k = k_n = k_p$ and $V_T = V_{T,n} = |V_{T,p}|$, and with a very small capacitive load. If the inverter is driven with an input voltage waveform with equal rise and fall times ($t = t_{rise} = t_{fall}$), it can be derived that the time-averaged short circuit current drawn from the power supply is

$$I_{avg}(short - circuit) = \frac{1}{12} \cdot \frac{k \cdot \tau \cdot f_{CLK}}{V_{DD}} (V_{DD} - 2V_T)^3$$

Hence, the short-circuit power dissipation becomes

$$P_{avg}(short - circuit) = \frac{1}{12} \cdot k \cdot \tau \cdot f_{CLK} \cdot (V_{DD} - 2V_T)^3$$

Note that the short-circuit power dissipation is linearly proportional to the input signal rise and fall times, and also to the transconductance of the transistors. Hence, reducing the input transition times will obviously decrease the short circuit current component.

