You should note that there will be different design criteria for each case, but you can still use the same basic loop topology and analysis methods.

2. Phase detector: compares the phase at each input and generates an error signal, $v_e(t)$, proportional to the phase difference between the two inputs. K_D is the gain of the phase detector (V/rad).

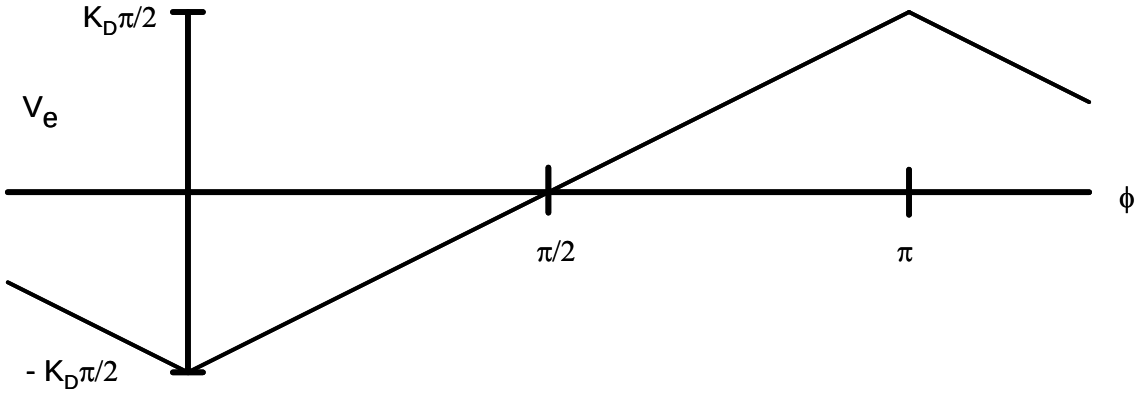
$$v_e(t) = K_D[\phi_{out}(t) - \phi_{in}(t)]$$

As one familiar circuit example, an analog multiplier or mixer can be used as a phase detector. Recall that the mixer takes the product of two inputs. $v_e(t) = A(t)B(t)$. If,

$$A(t) = A\cos(\omega_0 t + \phi_A)$$
$$B(t) = B\cos(\omega_0 t + \phi_B)$$
$$\text{Then,}\quad A(t)B(t) = (AB/2)[\cos(2\omega_0 t + \phi_A + \phi_B) + \cos(\phi_A - \phi_B)]$$

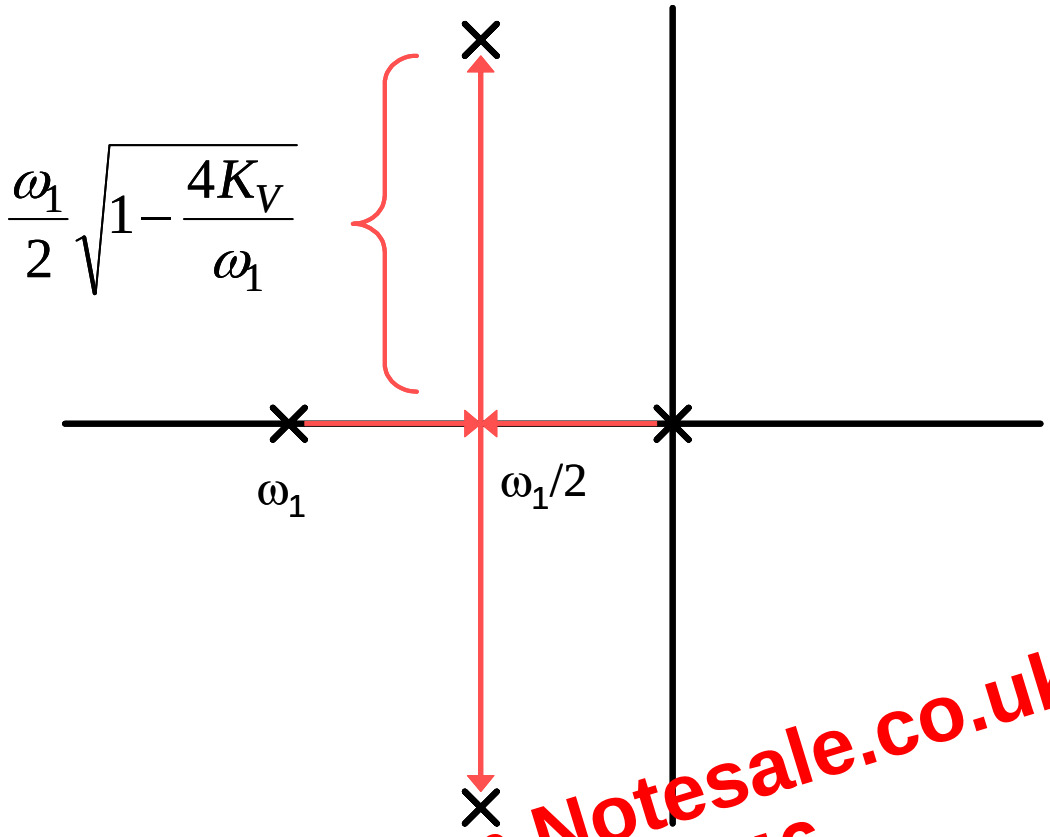
Since the two inputs are at the same frequency when the loop is locked, we have one output at twice the input frequency and an output proportional to the cosine of the phase difference. The doubled frequency component must be removed by the low pass loop filter. Any phase difference then shows up as the control voltage to the VCO, a DC or slowly varying AC signal after filtering.

The averaged transfer characteristic of such a phase detector is shown below. Note that in many implementations, the characteristic may be shifted up in voltage (single supply/single ended).



If the phase difference is $\pi/2$, then the average or integrated output from the XOR-type phase detector will be zero (or VDD/2 for single supply, digital XOR). The slope of the characteristic in either case is K_D.

3. VCO. In PLL applications, the VCO is treated as a linear, time-invariant system. Excess phase of the VCO is the system output.



We can have a very underdamped response when $\omega_1 << K_V$. Think about the inverse Laplace transform of the complex conjugate pole pair.

$$e^{-\omega_1 t/2}\sin\left(\frac{\omega_1}{2}\sqrt{1-\frac{4K_V}{\omega_1}}\right)t$$

There is an exponentially decaying term determined by the real part of the roots that shows how long it takes the system to settle after a phase or frequency step and a ringing frequency dictated by the imaginary part of the pole pair. Again, when $\omega_1 << K_V$, we have a high ringing frequency and a long settling time, characteristic of a system that is not very useful.

It is sometimes useful to define a natural frequency, ω_n, and a damping factor, ζ. This is standard control system terminology for a second order system. The key is to put the denominator of the closed loop transfer function, 1 + T(s), into a "standard" form: either

$$s^2 + 2\zeta\omega_n s + \omega_n^2$$

or

These parameters will have a strong effect on the loop dynamics which control overshoot and settling time. From the system design perspective, overshoot can be quite harmful, since it will cause the frequency to temporarily exceed the steady state value. Thus, the output of the synthesizer might land in an adjacent channel during part of the transient response. Settling time can also be critical since many TDM applications use different receive and transmit frequencies. The settling time determines how long you must wait until transmitting or receiving after a hop in frequency.

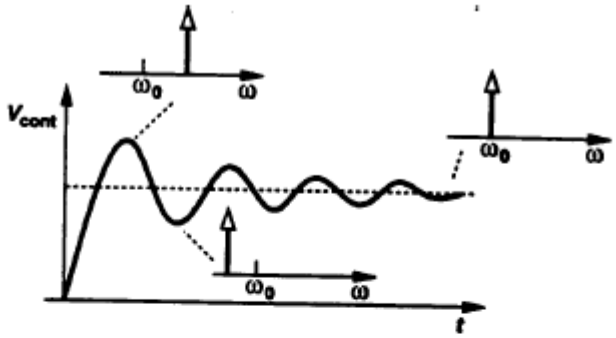


Figure 8.33 Variation of VCO frequency during synthesizer settling.

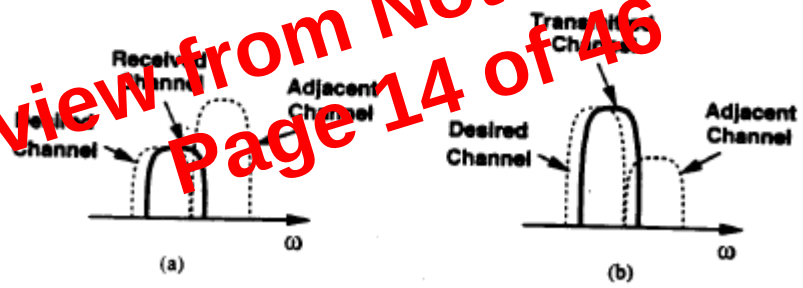
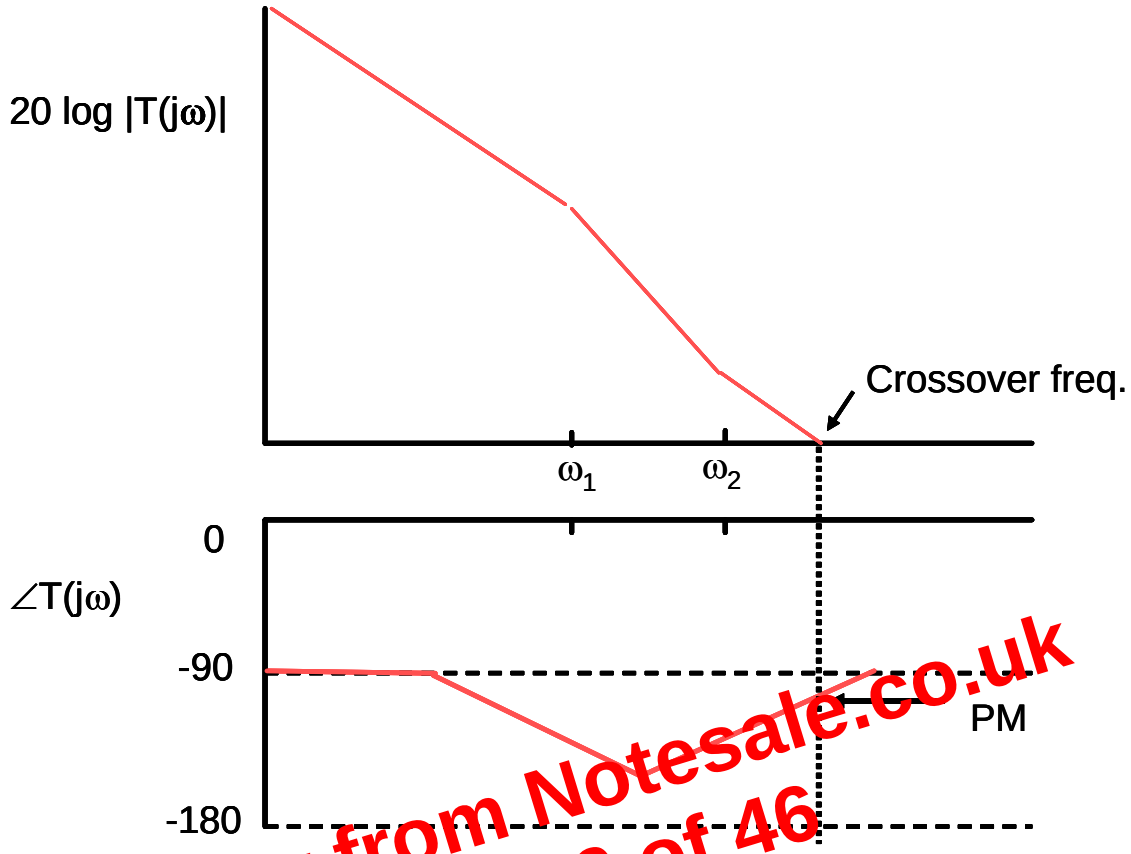


Figure 8.34 Effect of synthesizer settling on received and transmitted channels.

Ref. B. Razavi, RF Microelectronics, Prentice-Hall, 1998.

Here you see the consequences of PLL settling time if the PLL is being used as a local oscillator for a receiver or transmitter.



Note that the phase margin has increased. Now, small values of ω_1 can be used for narrower filter bandwidth, or higher K_V values can be used for lower phase error without sacrificing phase margin. Note how phase margin now improves when the crossover frequency is increased due to higher gain.

Root Locus: Calculate the closed loop transfer function for this PLL with the pole-zero loop filter.

$$\frac{\phi_o}{\phi_{in}} = \frac{(1+s/\omega_2)}{\frac{s^2}{K_V\omega_1} + s\left(\frac{1}{K_V} + \frac{1}{\omega_2}\right) + 1}$$

The denominator is of the form 1 + T(s). We can also extract ω_n and ζ from the closed loop transfer function since the denominator is in one of the standard forms.

$$H(s) = \frac{\phi_{out}}{\phi_{in}} = \frac{K_D K_O F(s)/s}{1 + K_D K_O F(s)/s}$$

$$H(s) = \frac{(1 + s/\omega_2)}{\frac{s^2}{K_D K_O \omega_1} + \frac{s}{\omega_2} + 1}$$

Thus, we can see that

$$\omega_n = \sqrt{K_D K_O \omega_1}$$

$$\varsigma = \frac{\omega_n}{2\omega_2}$$

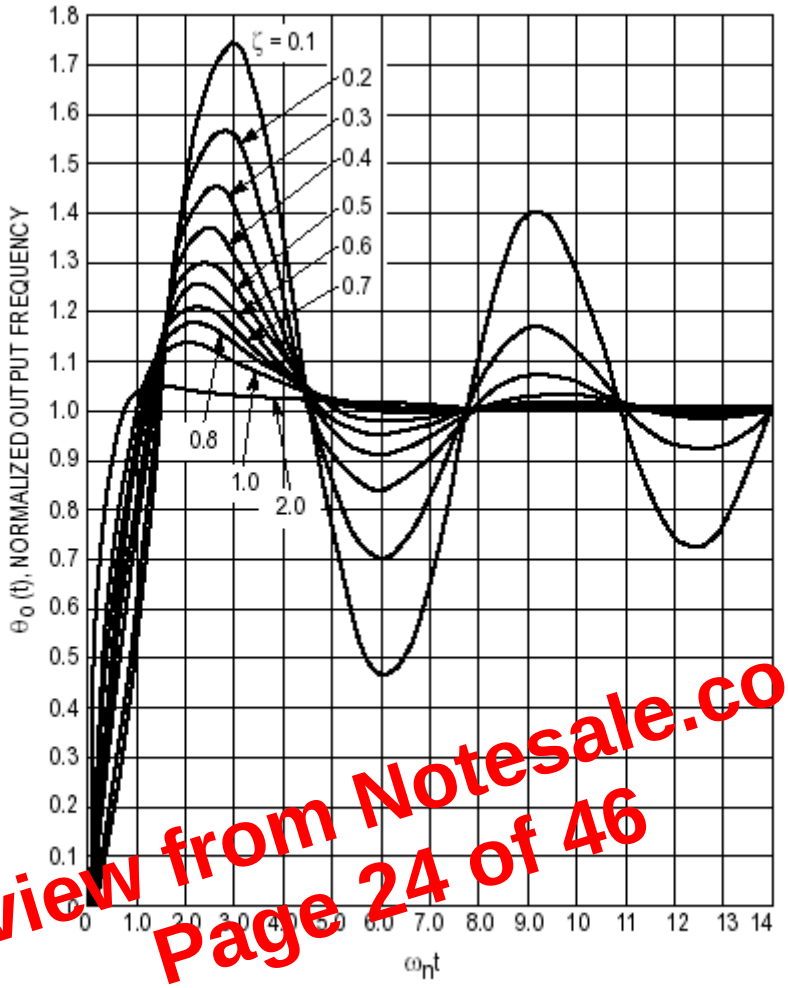


Figure 6. Type 2 Second Order Step Response

Ref. Motorola AN535

Here we see the phase and frequency step response for a type 2 PLL in terms of the key loop parameters. The settling time can be determined by setting an error tolerance around θo(t) = 1. For example, if settling to 5% were the criteria and if $\zeta = 1$, the response first falls within the boundary of 0.95 or 1.05 for $\omega_n t = 4.5$. Then settling time t can be determined since natural frequency ω_n will also be known.

Phase Frequency Detector

The phase-frequency detector shown below is a widely used architecture in frequency synthesizers. As opposed to the XOR phase detector that we first considered, this one produces two outputs: QA and QB, or as is customary, UP and DOWN respectively.

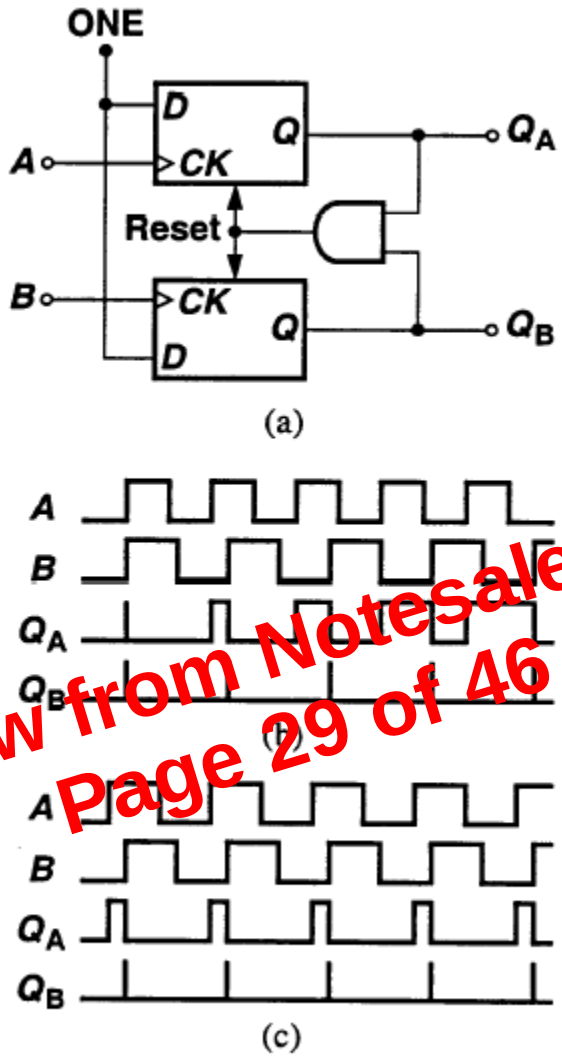


Figure 3.26. (a) Phase/frequency detector. Circuit response with (b) $\omega_A \geq \omega_B$, (A leading B.

Ref. J. Savoj and B. Razavi, High Speed CMOS for Optical Receivers, Kluwer Academic Publishing, 2001. (and many other books)

This phase detector has a much larger phase range (4π) of operation, and it will produce an output that drives the frequency in the right direction when it is out of lock. It also has zero offset when the phases are aligned and is insensitive to the duty cycle of the inputs since edge-triggered flip-flops are used.