## General Purpose Registers

• Each of these 26-bit registers are further subdivided into two 8-bit registers.

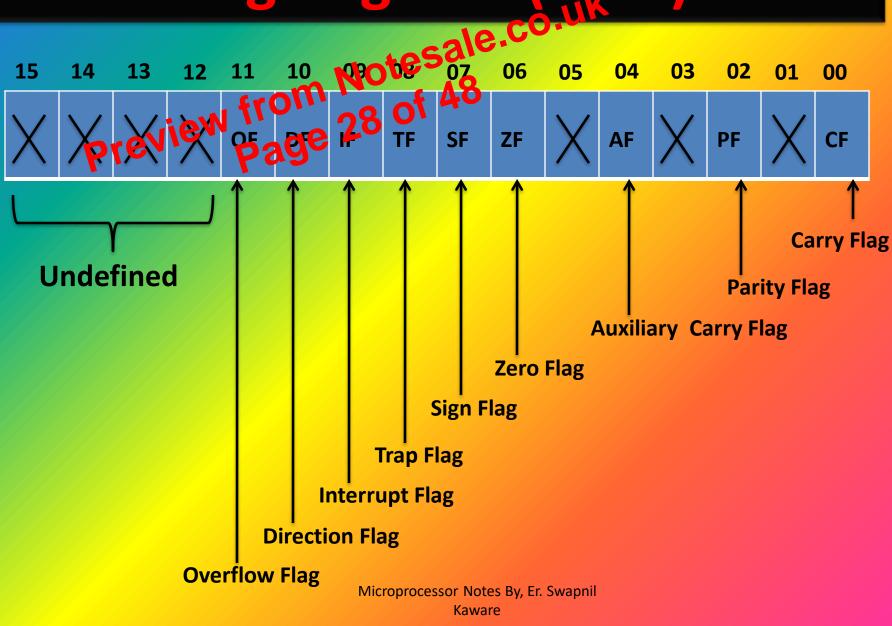
AX	
BX	
СХ	
DX	

AH	AL
BH	BL
СН	CL
DH	DL

## Pointer & Index Register

- Following to yange sters are under this category:
- (1). Stack Pointer (SP),
- (2). Base Pointer (BP),
- (3). Source Index (SI),
- (4). Destination Index (DI).

### Flag Register (PSW)



# Flag Register (RSW) Soar Pais 9 Plags and they are divided into two categories:

• (1). Condition Flags,

• (2). Control Flags.

Flag Register (PSW) • Following are the notes ale - Co-Preview page

<b>Condition Flags</b>	Control Flags
1. Carry Flag	1. Trap Flag
2. Auxiliary Carry Flag	2. Interrupt Flag
3. Zero Flag	3. Directional Flag
4. Sign Flag	
5. Parity Flag	
6. Overflow Flag	

## Flag Register (PSW)

- Carry Flag (CY): This flag indicates an overflow condition for unsigned integer arthmetic of is also used in multipleprecision althmetiage
- Auxiliary Flag (AC): If an operation performed in ALU generates a carry/barrow from lower nibble (i.e. D0 – D3) to upper nibble (i.e. D4 – D7), the AC flag is set i.e. carry given by D3 bit to D4 is AC flag. This is not a general-purpose flag, it is used internally by the processor.
- Parity Flag (PF): This flag is used to indicate the parity of result. If lower order 8-bits of the result contains even number of 1's, the Parity Flag is set and for odd number of 1's, the Parity flag is reset.

## Signals In Minimum Mode

(9). INTR: (Interrupt request) of 40 availability of request). 43 of 40 (10). INTA: when goes low processor acknowledges the interrupt.

(11). TEST: Processor suspends operation when goes high & resumes the operation when goes low. It is used to synchronize the processor to external events.

(12). NMI: (Non Maskable interrupt): it can not be delayed or rejected i.e. can not be recognized.

(13). RESET: when goes low processor terminates the current activity & goes to reset state.

## Signals In Maximum Mode

(17). S2, S1, S0 – Statul Ones, These are the status lines which reflect the type 45 operation, being carried out by the processor.

<b>SO</b>	S1	S2	Indication
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O port
0	1	0	Write I/O port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

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