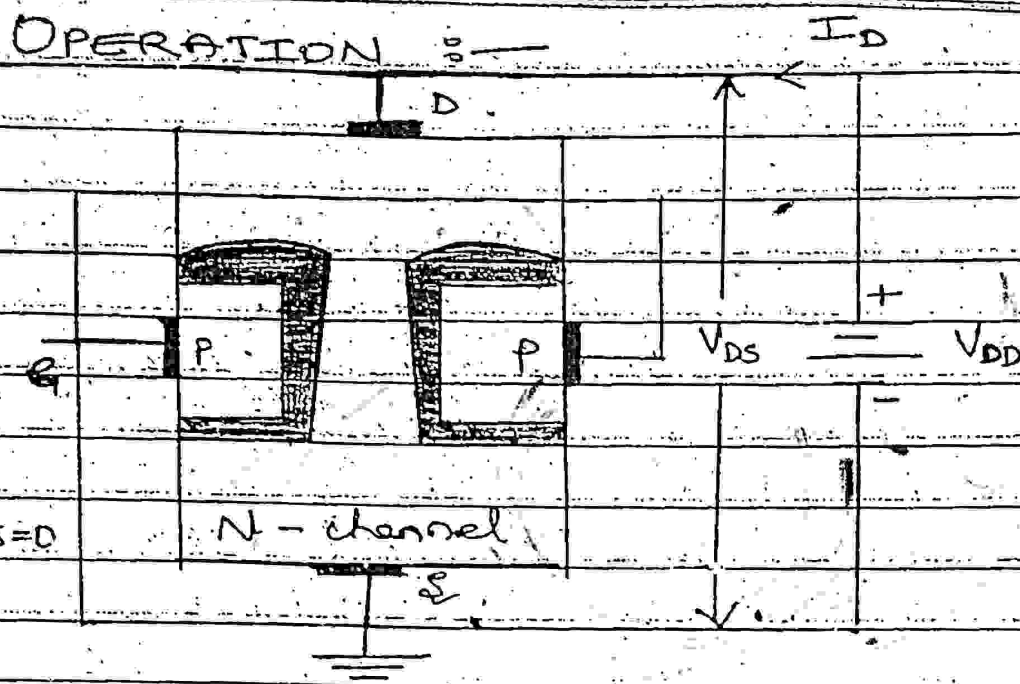




(i) When $V_{GS} = 0$, & $V_{DS} > 0$ (same +ve volt)

- (*) When voltage is applied between the drain & source with DC supply V_{DS} , electrons flow from source to drain through the narrow channel existing between depletion region.
- (*) When $V_{GS} = 0$ & $V_{DS} > 0$, the PN junctions are reverse biased. Because of reverse biasing, depletion region widens at the D end of channel, & reduces towards the S end.
- (*) As V_{DS} is increased from zero, I_D increases. As the channel width starts decreasing between source (S) to drain (D), current I_D saturates.

(ii) As $V_{GS} < 0$ (-ve volt)

- (*) A voltage source is connected between the gate (G) & source (S) terminals as V_{GS} , which is negative. When the G to S voltage V_{GS} is increased with negative value, reverse bias across Gate to source also increases. This reduces the width of depletion channel, & thus