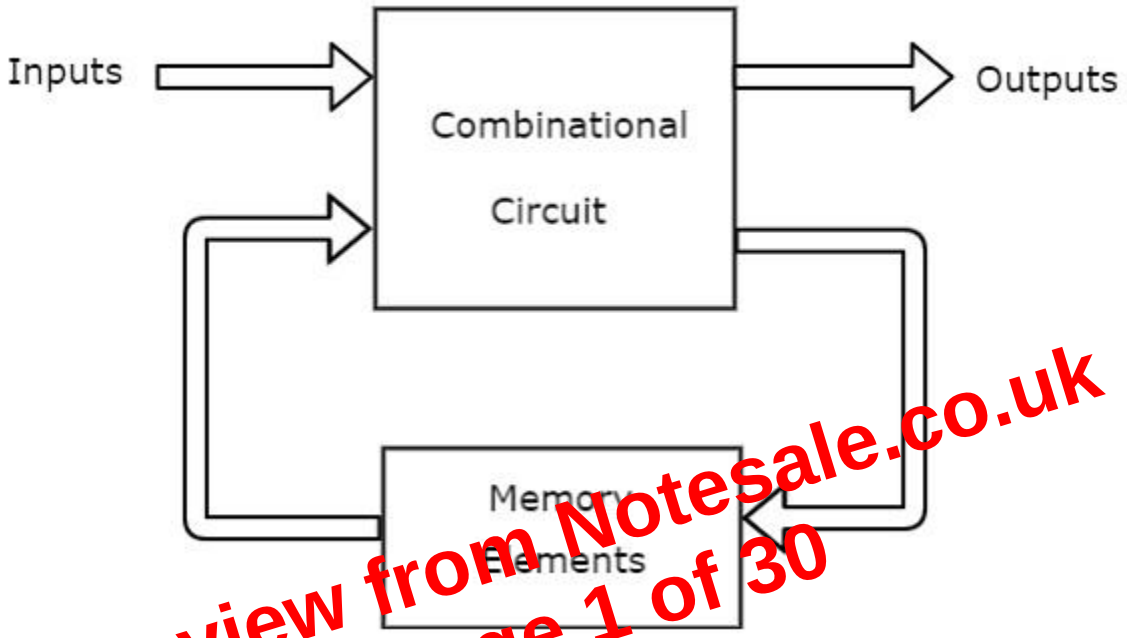
Digital Sequential Circuits

We covered numerous combinational circuits in earlier chapters. These circuits each have a set of outputs that depend exclusively on the configuration of the available inputs. The accompanying graphic shows the block diagram for a sequential circuit.

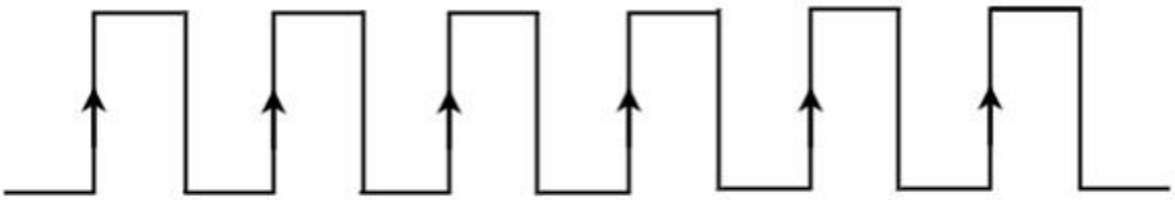


This sequential circuit has a number of inputs and outputs. The sum of the current inputs and the previous outputs have an impact on the sequential circuit's outputs. Nothing more than the previous output exists in the present state. As a result, sequential circuits have both combinational circuits and memory storage components. Some sequential circuits don't even have combinational circuits; they merely have memory components.

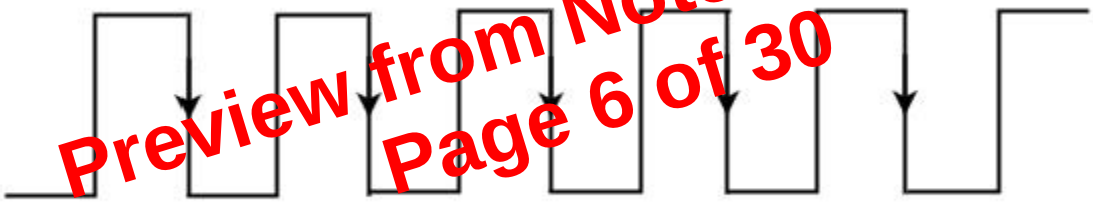
The differences between sequential and combinational circuits are shown in the following table.

Combinational Circuits	Sequential Circuits

If the sequential circuit is operated with the clock signal that is transitioning from Logic Low to Logic High, then that type of triggering is known as Positive edge triggering. It is also called as rising edge triggering. It is shown in the following figure.



If the sequential circuit is operated with the clock signal that is transitioning from Logic High to Logic Low, then that type of triggering is known as Negative edge triggering. It is also called as falling edge triggering. It is shown in the following figure.



In coming chapters, we will discuss about various sequential circuits based on the type of triggering that can be used in it.

Digital Circuits - Latches

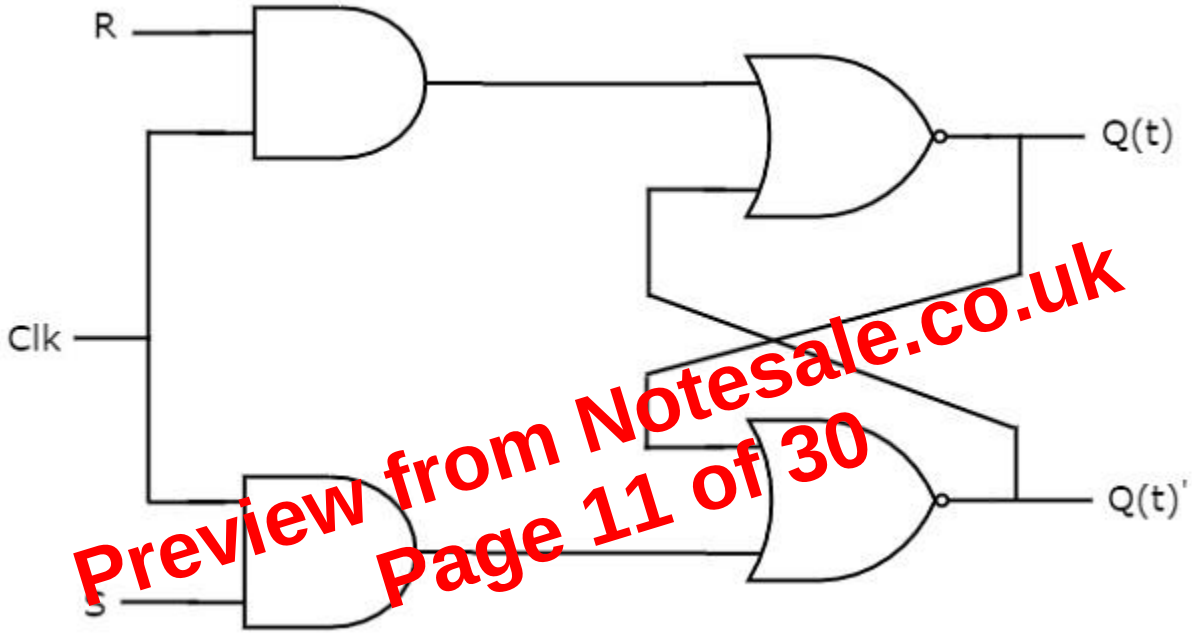
There are two types of memory elements based on the type of triggering that is suitable to operate it.

- Latches

- T Flip-Flop

SR Flip-Flop

SR flip-flop operates with only positive clock transitions or negative clock transitions. Whereas, SR latch operates with enable signal. The circuit diagram of SR flip-flop is shown in the following figure.

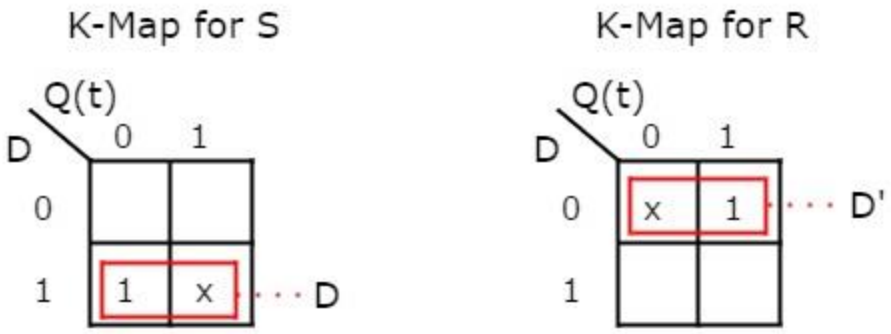


This circuit has two inputs S & R and two outputs Qtt & Qtt'. The operation of SR flipflop is similar to SR Latch. But, this flip-flop affects the outputs only when positive transition of the clock signal is applied instead of active enable.

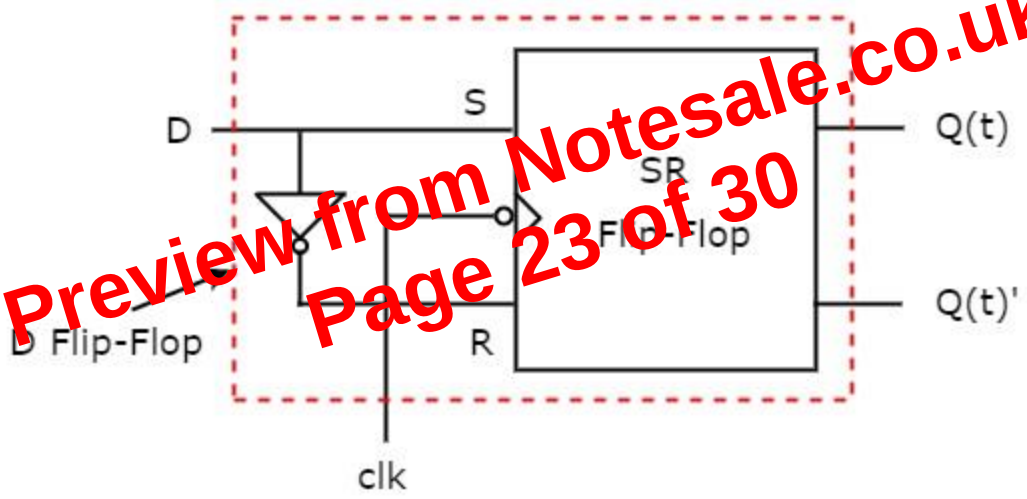
The following table shows the state table of SR flip-flop.

S	R	Qt+1t+1
0	0	Qtt

We can use 2 variable K-Maps for getting simplified expressions for these inputs. The k-Maps for S & R are shown below.



So, we got S = D & R = D' after simplifying. The circuit diagram of D flip-flop is shown in the following figure.



This circuit consists of SR flip-flop and an inverter. This inverter produces an output, which is complement of input, D. So, the overall circuit has single input, D and two outputs Qtt & Qtt'. Hence, it is a D flip-flop. Similarly, you can do other two conversions.

D Flip-Flop to other Flip-Flop Conversions

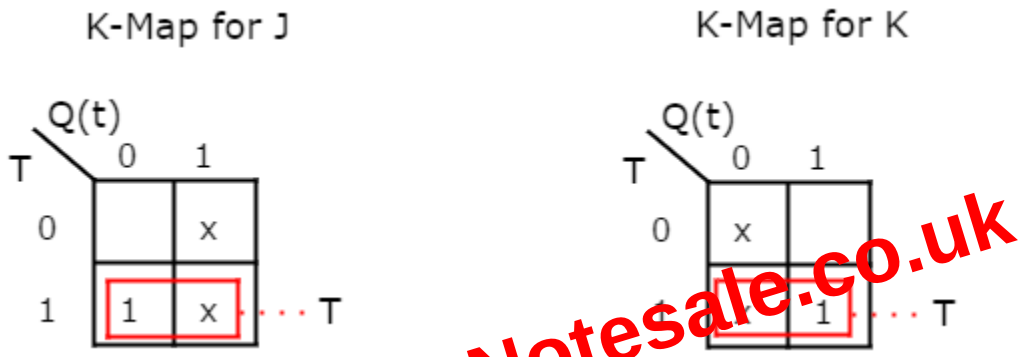
Following are the three possible conversions of D flip-flop to other flip-flops.

From the above table, we can write the Boolean functions for each input as below.

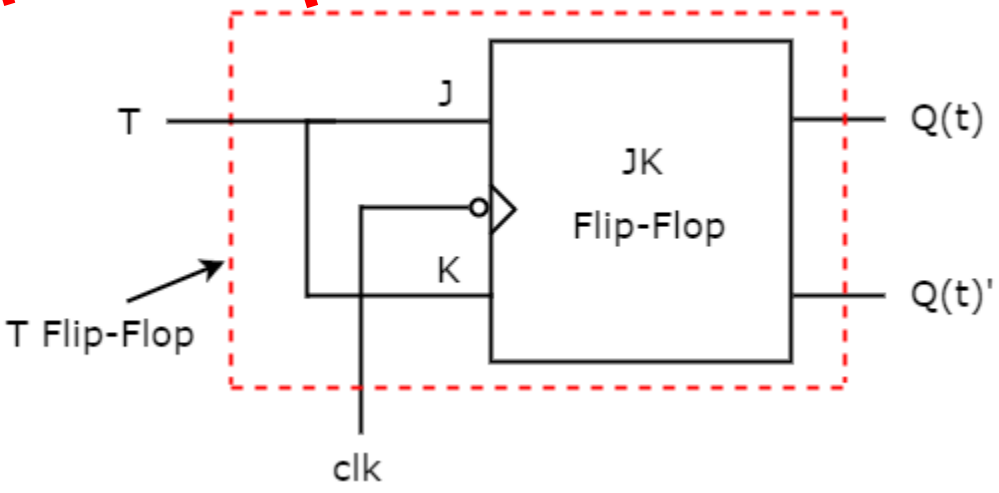
$$J=m2+d1+d3J=m2+d1+d3$$

$$K=m3+d0+d2K=m3+d0+d2$$

We can use 2 variable K-Maps for getting simplified expressions for these two inputs. The k-Maps for J & K are shown below.



So, we got, J = T & K = T after simplifying. The circuit diagram of T flip-flop is shown in the following figure.



This circuit consists of JK flip-flop only. It doesn't require any other gates. Just connect the same input T to both J & K. So, the overall circuit has single input, T and two outputs Qtt & Qtt'.