An ‘N’ bit binary counter consists of ‘N’ T flip-flops. If the counter counts from 0 to $2^N - 1$, then it is called as binary up counter. Similarly, if the counter counts down from $2^N - 1$ to 0, then it is called as binary down counter.

There are two types of counters based on the flip-flops that are connected in synchronous or not.

- Asynchronous counters
- Synchronous counters

Asynchronous Counters

If the flip-flops do not receive the same clock signal, then that counter is called as Asynchronous counter. The output of system clock is applied as clock signal only to first flip-flop. The remaining flip-flops receive the clock signal from output of its previous stage flip-flop. Hence, the outputs of all flip-flops do not change affectaffect at the same time.

Now, let us discuss the following two counters one by one.

- Asynchronous Binary up counter
- Asynchronous Binary down counter

Asynchronous Binary Up Counter

An ‘N’ bit Asynchronous binary up counter consists of ‘N’ T flip-flops. It counts from 0 to $2^N - 1$. The block diagram of 3-bit Asynchronous binary up counter is shown in the following figure.

Synchronous Counters

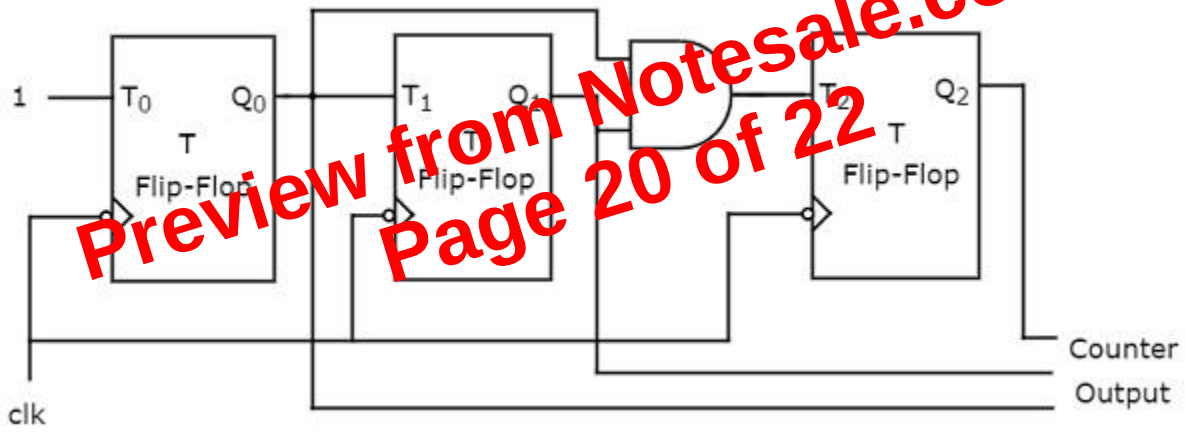
If all the flip-flops receive the same clock signal, then that counter is called as Synchronous counter. Hence, the outputs of all flip-flops change affectaffect at the same time.

Now, let us discuss the following two counters one by one.

- Synchronous Binary up counter
- Synchronous Binary down counter

Synchronous Binary Up Counter

An 'N' bit Synchronous binary up counter consists of 'N' T flip-flops. It counts from 0 to $2^N - 1$. The block diagram of 3-bit Synchronous binary up counter is shown in the following figure.



The 3-bit Synchronous binary up counter contains three T flip-flops & one 2-input AND gate. All these flip-flops are negative edge triggered and the outputs of flip-flops change affectaffect synchronously. The T inputs of first, second and third flip-flops are 1, Q0Q0 & Q1Q0Q1Q0 respectively.

The output of first T flip-flop toggles for every negative edge of clock signal. The output of second T flip-flop toggles for every negative edge of clock signal if Q0Q0 is 1. The output of third T