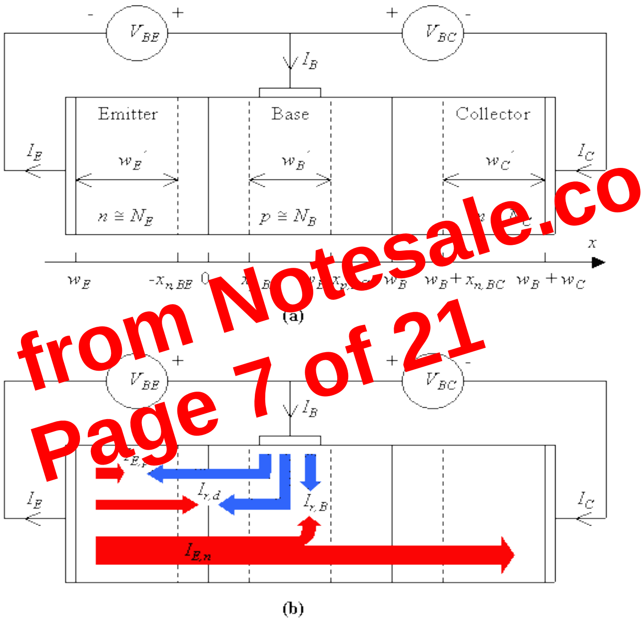
As you can see, the *controlling* current and the *controlled* current always mesh together through the emitter wire, and their electrons always flow *against* the direction of the transistor's arrow. This is the first and foremost rule in the use of transistors: all currents must be going in the proper directions for the device to work as a current regulator. The small, controlling current is usually referred to simply as the *base current* because it is the only current that goes through the base wire of the transistor. Conversely, the large, controlled current is referred to as the *collector current* because it is the only current that goes through the collector wire. The emitter current is the sum of the base and collector currents, in compliance with Kirchhoff's Current Law.

No current through the base of the transistor, shuts it off like an open switch and prevents current through the collector. A base current, turns the transistor on like a closed switch and allows a proportional amount of current through the collector. Collector current is primarily limited by the base current, regardless of the amount of voltage available to push it. The next section will explore in more detail the use of bipolar transistors as switching elements.

Structure and principle of operation

A bipolar junction transistor consists of two back-to-back p-n junctions, who share a thin common region with width, w_B. Contacts are made to all three regions, the two outer regions called the emitter and collector and the middle region called the base. The structure of an npn bipolar transistor is shown in figures below (a). The device is called “bipolar” since its operation involves both types of mobile carriers, electrons and holes.



(a) Structure and sign convention of an npn bipolar junction transistor.
(b) Electron and hole flow under forward active bias, $V_{BE} > 0$ and $V_{BC} = 0$.

Since the device consists of two back-to-back diodes, there are depletion regions between the quasi-neutral regions. The width of the quasi neutral regions in the emitter, base and collector are indicated with the symbols w_E', w_B' and w_C' and are calculated from

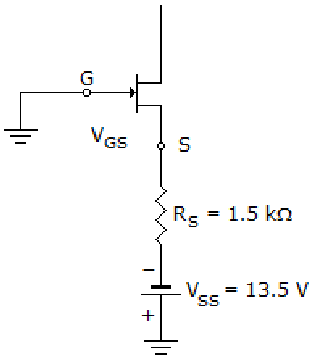
$$w_E' = w_E - x_{n,BE} \tag{5.2.1}$$

$$w_B' = w_B - x_{p,BE} - x_{p,BC} \tag{5.2.2}$$

$$w_C' = w_C - x_{n,BC} \tag{5.2.3}$$

where the depletion region widths are given by:

5. Calculate the value of V_{DS}.



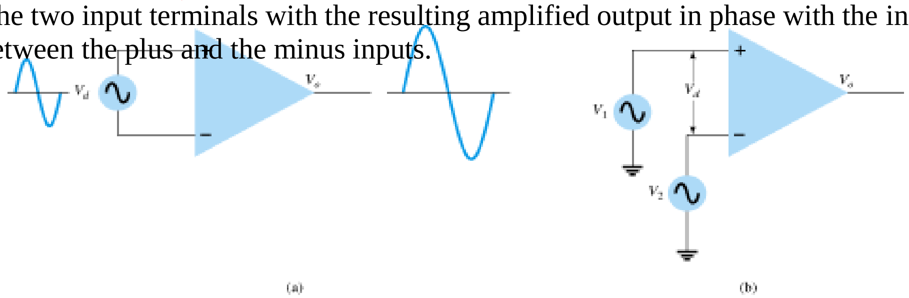
Part D – Operational Amplifier

Introduction – an operational amplifier, or op-amp, is a very high gain differential amplifier with high input impedance and low output impedance. Typical uses of the operational amplifier are to provide voltage amplitude changes (amplitude and polarity), oscillators, timer circuits, filter circuits, comparator and many types of instrumentation circuits. An op-amp contains a number of differential amplifier stages to achieve a very high voltage gain.

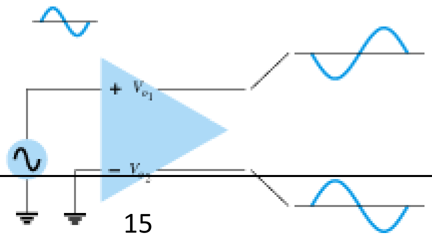
A basic op-amp has two inputs and one output as would result in using differential amplifier input stage. Each input results in either the same or an opposite polarity (or phase) output, depending on whether the signal is applied to the inverting (-) or the non-inverting (+) input, respectively.

1. **Single-ended Input** – when the input signal is connected to one input with the other input is connected to ground. The input is applied to the plus input (with minus input connected to the ground), which results in an output with having the same polarity as the applied input signal.

2. **Double-ended (Differential) Input** – In addition to using only one input, it is possible to apply signals at each input. In the figure below is a double-ended input operation where the input, applied between the two input terminals with the resulting amplified output in phase with the input signals applied between the plus and the minus inputs.



3. **Double-Ended Output** – the op-amp can also be operated with opposite outputs as shown in the figure below. An input signal applied to either input will result in outputs from both output terminal, these outputs always being opposite in polarity. The reference output is also referred to as a floating signal since neither output terminal is ground (reference) terminal. The output is twice as large as either of the two output voltage value because they are of opposite polarity and subtracting those results in twice their amplitude.



1. **Input offset voltage (V_{IO}):** the input offset voltage is seen to be typically 1 mV, but can go as high as 6 mV. The output offset is then computed based on the circuit used. If the worst condition possible is of interest, the maximum value should be used. Typical values are those more commonly expected when using the op-amp.
2. **Input offset current (I_{IO}):** the input offset current is listed to be typically 20 nA, whereas the largest value expected is 200 nA.
3. **Input bias current (V_{ICR}):** it is typically 80 nA and may be as large as 500 nA.
4. **Common-**mode input voltage range (VICB): this parameter lists the range over which the input voltage may vary (using a supply of ±15 V), about ±12 V to ±13 Inputs larger in amplitude than this value will probably result in output distortion and should be avoided.
5. **Maximum peak output voltage swing (V_{OM}):** this parameter lists the largest amount the output may vary (using ± 15 V supply). Depending on the circuit closed-loop gain, the input signal should be limited to keep the output from varying by an amount larger than ±12 V.
6. **Large signal voltage amplification (A_{VD}):** this is the open-loop voltage gain of the op-amp. Although a minimum value of 20 V/mV, or 20, 000 V/V is listed, the manufacturer also list a typical value of 200 V/mV or 200, 000 V/V.\
7. **Input Resistance (r_i):** the input resistance of an op-amp when measured under open-loop condition is typically 2 MΩ, but could be as little as 300 kΩ. In a closed-loop circuit, this input impedance can be much larger.
8. **Output resistance (r_o):** the op-amp output resistance is listed as typically 75 Ω. No minimum or maximum value is given by the manufacturer. In closed-loop circuit, the output impedance can be lower depending on the gain.
9. **Input capacitance (C_I):** for high frequency considerations, it is helpful to know that the input to the op-amp has typically 1.4 pF of capacitance. An even small value compared to the stray wiring.
10. **Supply current (I_{CC}):** the op-amp draws a total of 2.8 mA, typically from the dual voltage supply, but the current drawn could be as little as 1.7 mA. This parameters helps the user determine the size of the voltage supply to use, it can also be used to calculate the power dissipated by the IC ($P_D = 2\ V_{CC}I_{CC}$).
11. **Common-mode rejection ratio (CMRR):** the parameter is seen to be 90 dB, but could go as low as 70 dB. Since 90 dB is equivalent to 31,622.78, the op-amp amplifies noise (common inputs) by almost 30, 000 times less than the difference inputs.
12. **Total power dissipation (P_D):** it is typically 50 mW but could go as high as 85 mW.

Reading List

[1] Jaeger & Blalock, Microelectronic Circuit Design (4th edition), McGraw Hill, 2010.
[2] Pierret, Semiconductor Device Fundamentals, Addison Wesley, 1996, ISBN 0201543931
[3] http://www.ece.gatech.edu/academics/courses/course_outline.php?prmCourse=ECE3040
[4] http://en.wikipedia.org/wiki/Operational_Amplifier