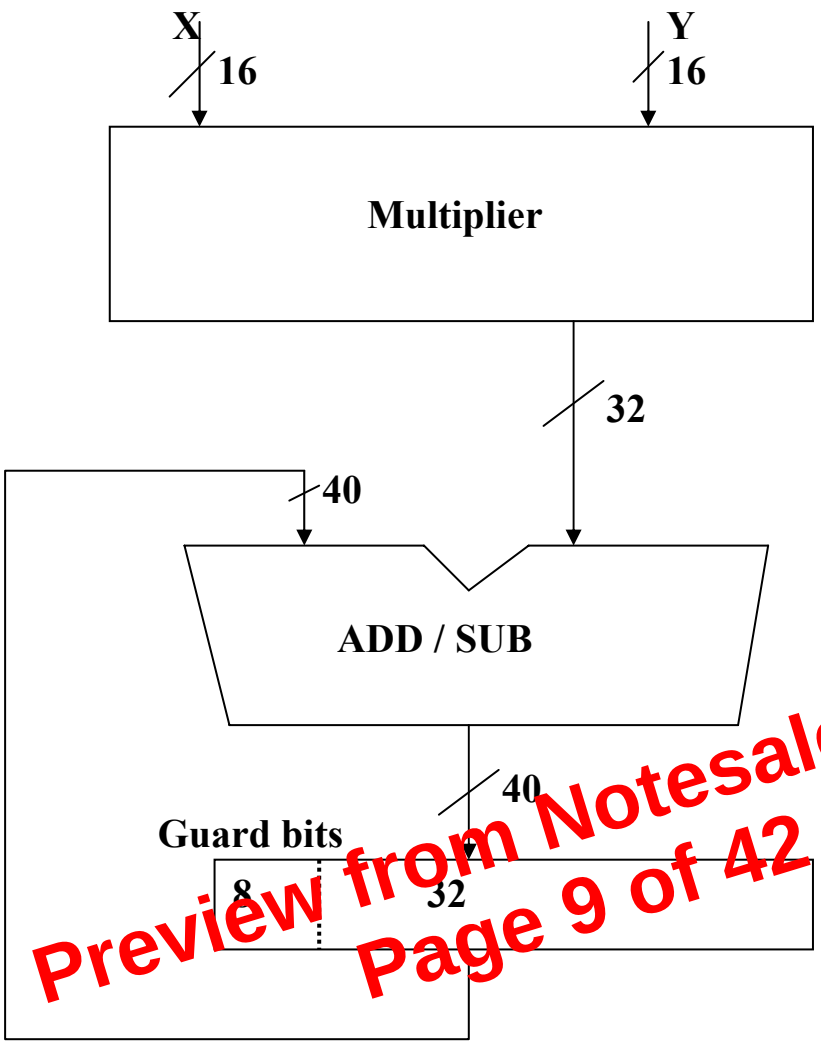
- Computers can be generally classified by size and power as follows, though there is considerable overlap:
- **Personal computer**: A small, single-user computer based on a microprocessor.
- In addition to the microprocessor, a personal computer has a keyboard for entering data, a monitor for displaying information, and a storage device for saving data.
- **Working station**: A powerful, single-user computer. A workstation is like a personal computer, but it has a more powerful microprocessor and a higher-quality monitor.
- **Minicomputer**: A multi-user computer capable of supporting from 10 to hundreds of users simultaneously.
- **Mainframe**: A powerful multi-user computer capable of supporting many hundreds or thousands of users simultaneously.
- **Supercomputer:** An extremely fast computer that can perform hundreds of millions of instructions per second.

Minicomputer:

- A midsized computer. In size and power, minicomputers lie between workstations and mainframes.
- A minicomputer, a term no longer much used, is a computer of a size intermediate between a microcomputer and a mainframe.
- Typically, minicomputers have been stand-alone computers (computer systems with attached terminals and other devices) sold to small and mid-size businesses for general business applications and to large enterprises for department-level operations.
- In recent years the minicomputer has evolved into the "mid-range server" and is part of a network. IBM's AS/400e is a good example.
- The AS/400 - formally renamed the "IBM iSeries," but still commonly known as AS/400 - is a midrange server designed for small businesses and departments in large enterprises and now redesigned so that it will work well in distributed networks with Web applications.
- The AS/400 uses the PowerPC microprocessor with its reduced instruction set computer technology. Its operating system is called the OS/400.
- With multi-terabytes of disk storage and a Java virtual memory closely tied into the operating system, IBM hopes to make the AS/400 a kind of versatile all-purpose server that can replace PC servers and Web servers in the world's businesses, competing with both Wintel and Unix servers, while giving its present enormous customer base an immediate leap into the Internet.

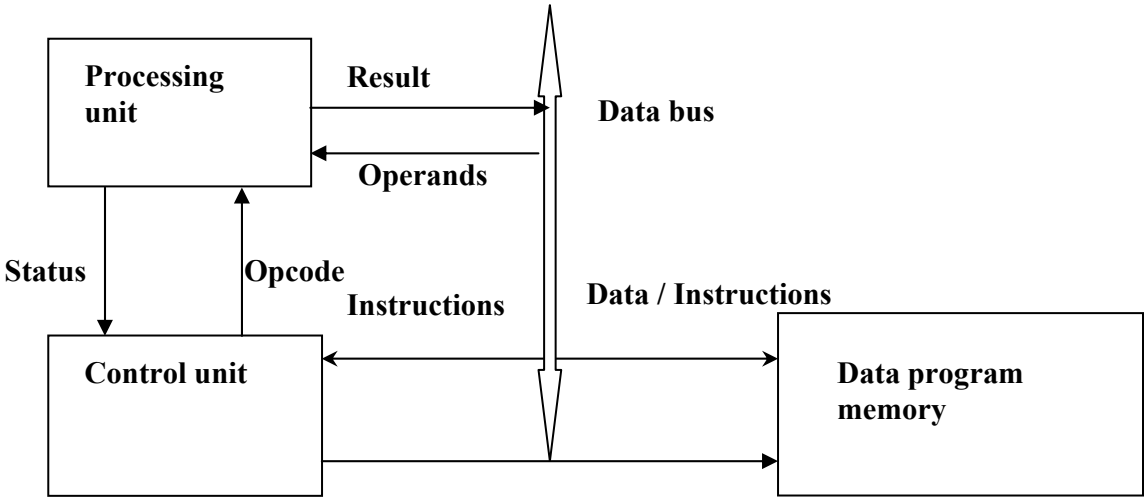
Workstation:

1) A type of computer used for engineering applications (CAD/CAM), desktop publishing, software development, and other types of applications that require a moderate amount of computing power and relatively high quality graphics capabilities.
- Workstations generally come with a large, high- resolution graphics screen, at least 64 MB (mega bytes) of RAM, built-in network support, and a graphical user interface.

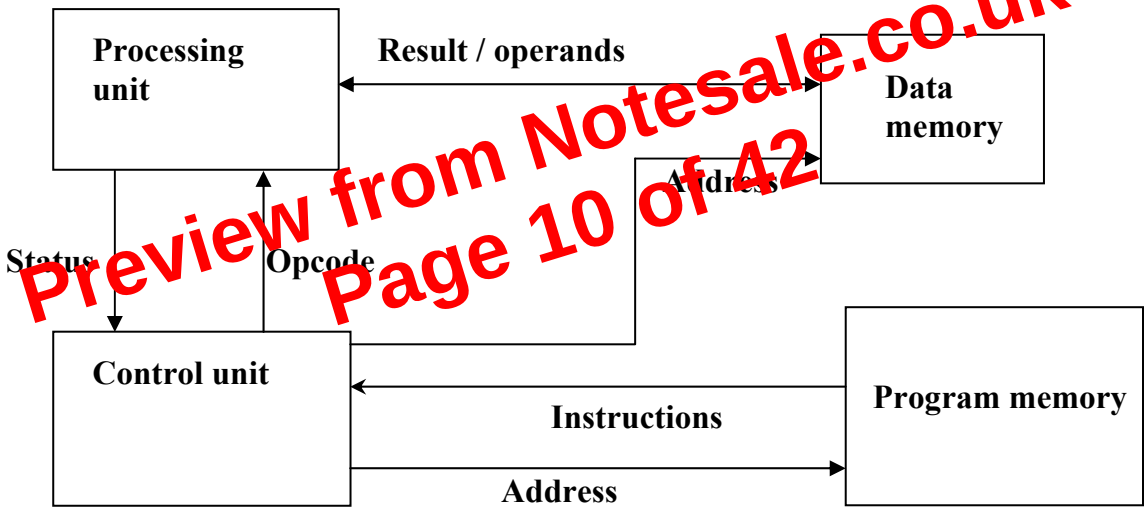


A MAC unit with accumulator guard bits

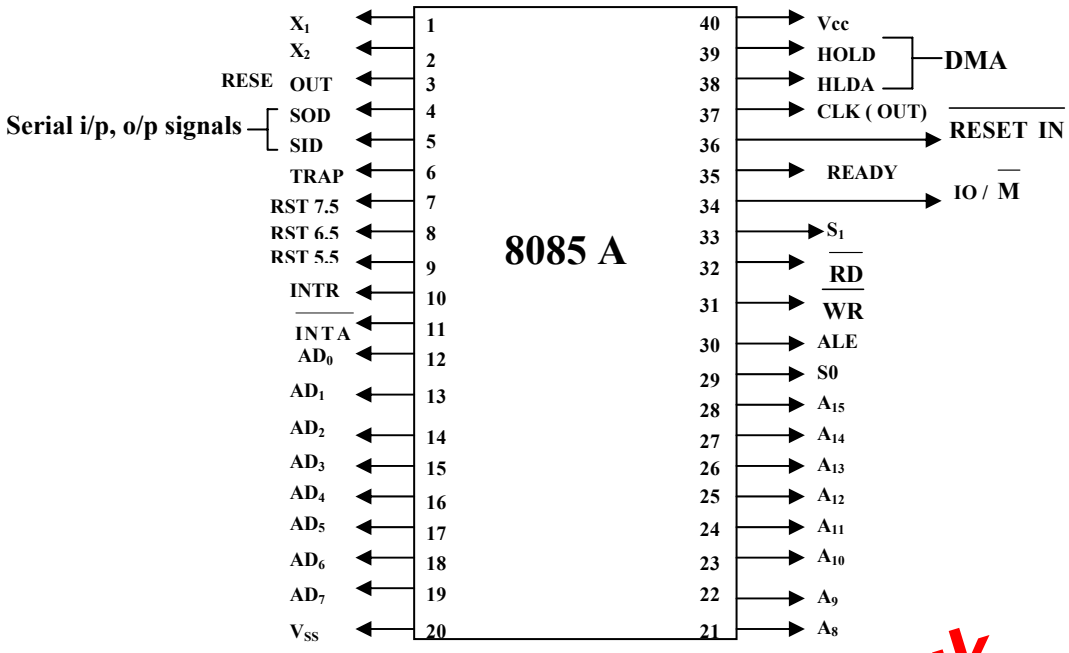
- The processor core connects to these memory spaces by two separate bus sets, allowing two simultaneous access to memory. This arrangement doubles the processor memory bandwidth.
-
- ***Zero-overhead looping***: one common characteristics of DSP algorithms is that most of the processing time is split on executing instructions contained with relatively small loops.
- The term zero overhead looping means that the processor can execute loops without consuming cycles to test the value of the loop counter, perform a conditional branch to the top of the loop, and decrement the loop counter.



Von Neuman Architecture

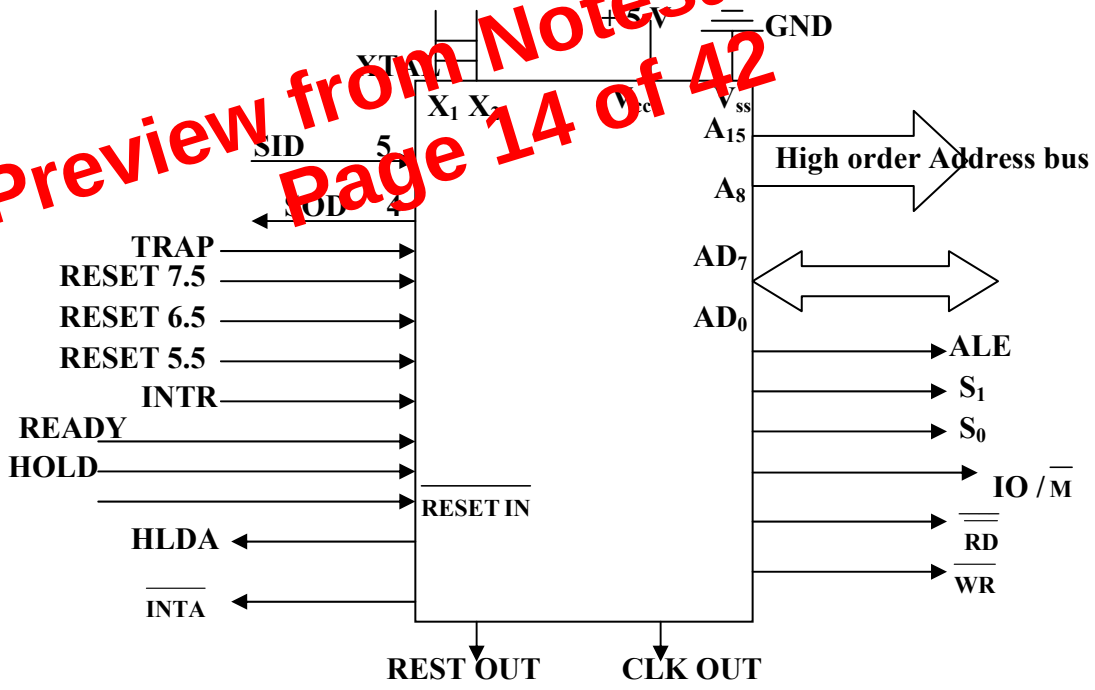


Harvard Architecture

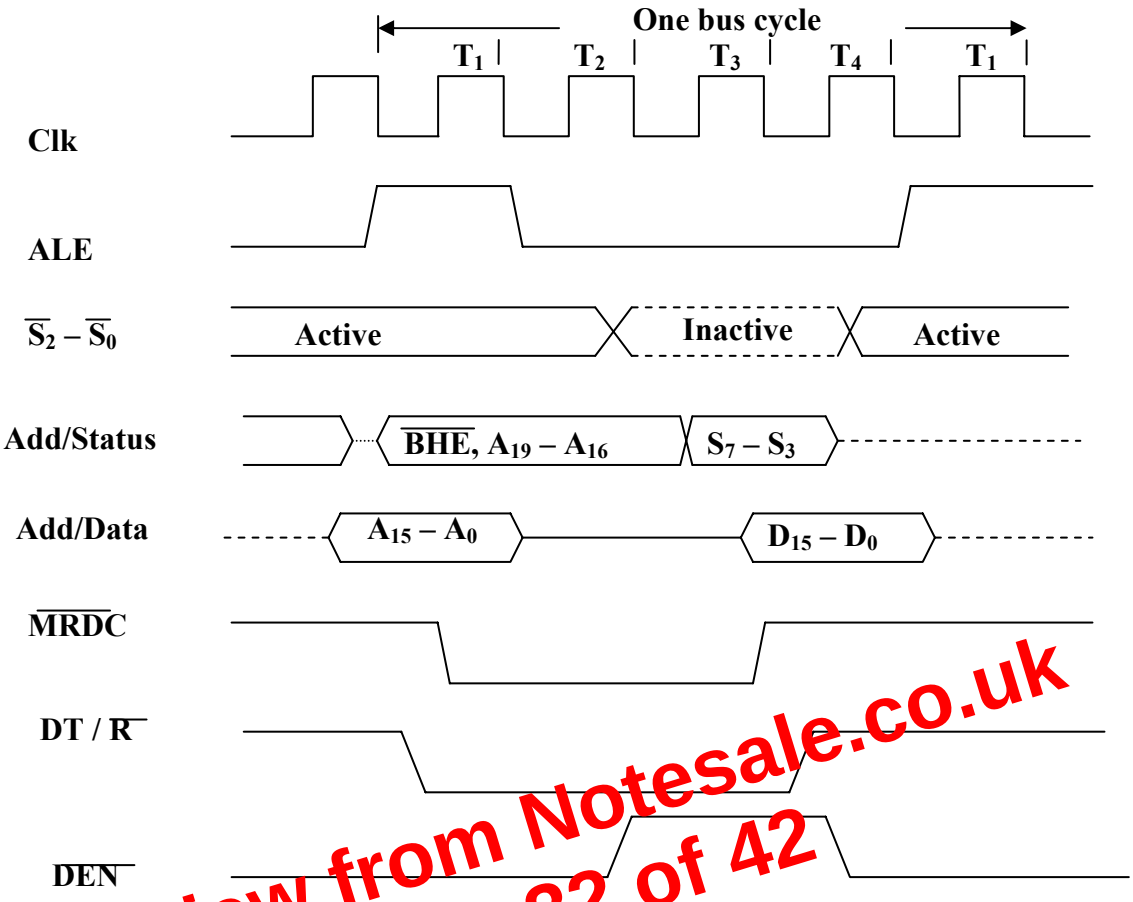


Pin Diagram of 8085

Signal Groups of 8085



•**READY**: This is the acknowledgement from the slow device or memory that they have completed the data transfer. The signal made available by the devices is synchronized by the 8284A clock generator to provide ready input to the 8086. the signal is active high.
•**INTR-Interrupt Request**: This is a triggered input. This is sampled during the last clock cycles of each instruction to determine the availability of the request. If any interrupt request is pending, the processor enters the interrupt acknowledge cycle.
•This can be internally masked by resulting the interrupt enable flag. This signal is active high and internally synchronized.
• $\overline{\textbf{TEST}}$ This input is examined by a 'WAIT' instruction. If the TEST pin goes low, execution will continue, else the processor remains in an idle state. The input is synchronized internally during each clock cycle on leading edge of clock.
•**CLK**- Clock Input: The clock input provides the basic timing for processor operation and bus control activity. Its an asymmetric square wave with 33% duty cycle.
•**MN/** $\overline{\textbf{MX}}$: The logic level at this pin decides whether the processor is to operate in either minimum or maximum mode.
•**The following pin functions are for the minimum mode operation of 8086.**
•**M/** $\overline{\textbf{IO}}$ **– Memory/IO**: This is a status line logically equivalent to S_2 in maximum mode. When it is low, it indicates the CPU is having an I/O operation, and when it is high, it indicates that the CPU is having a memory operation. This line becomes active high in the previous T_4 and remains active till final T_4 of the current cycle. It is tristated during local bus "hold acknowledge ".
• $\overline{\textbf{INTA}}$ **Interrupt Acknowledge**: This signal is used as a read strobe for interrupt acknowledge cycles. i.e. when it goes low, the processor has accepted the interrupt.
•**ALE – Address Latch Enable**: This output signal indicates the availability of the valid address on the address/data lines, and is connected to latch enable input of latches. This signal is active high and is never tristated.
•**DT/** $\overline{\textbf{R}}$ **– Data Transmit/Receive**: This output is used to decide the direction of data flow through the transreceivers (bidirectional buffers). When the processor sends out data, this signal is high and when the processor is receiving data, this signal is low.
•**DEN – Data Enable**: This signal indicates the availability of valid data over the address/data lines. It is used to enable the transreceivers (bidirectional buffers) to separate the data from the multiplexed address/data signal. It is active from the middle of T_2 until the middle of T_4. This is tristated during ' hold acknowledge' cycle.
•**HOLD, HLDA- Acknowledge**: When the HOLD line goes high, it indicates to the processor that another master is requesting the bus access.
•The processor, after receiving the HOLD request, issues the hold acknowledge signal on HLDA pin, in the middle of the next clock cycle after completing the current bus cycle.•At the same time, the processor floats the local bus and control lines. When the processor detects the HOLD line low, it lowers the HLDA signal. HOLD is an asynchronous input, and is should be externally synchronized.
•If the DMA request is made while the CPU is performing a memory or I/O cycle, it will release the local bus during T_4 provided:
1.The request occurs on or before T_2 state of the current cycle.
2.The current cycle is not operating over the lower byte of a word.
3.The current cycle is not the first acknowledge of an interrupt acknowledge sequence.



Memory Read Timing in Maximum Mode

•**INTR** is a maskable hardware interrupt. The interrupt can be enabled/disabled using STI/CLI instructions or using more complicated method of updating the FLAGS register with the help of the POPF instruction.
•When an interrupt occurs, the processor stores FLAGS register into stack, disables further interrupts, fetches from the bus one byte representing interrupt type, and jumps to interrupt processing routine address of which is stored in location 4 * <interrupt type>. Interrupt processing routine should return with the IRET instruction.
•**NMI** is a non-maskable interrupt. Interrupt is processed in the same way as the INTR interrupt. Interrupt type of the NMI is 2, i.e. the address of the NMI processing routine is stored in location 0008h. This interrupt has higher priority then the maskable interrupt.
•**Software interrupts** can be caused by:
•INT instruction - breakpoint interrupt. This is a type 3 interrupt.
•INT <interrupt number> instruction - any one interrupt from available 256 interrupts.
•INTO instruction - interrupt on overflow
•Single-step interrupt - generated if the TF flag is set. This is a type 1 interrupt. When the CPU processes this interrupt it clears TF flag before calling the interrupt processing routine.
•**Processor exceptions**: Divide Error (Type 0), Unused Opcode (type 6) and Escape opcode (type 7).
•Software interrupt processing is the same as for the hardware interrupts.