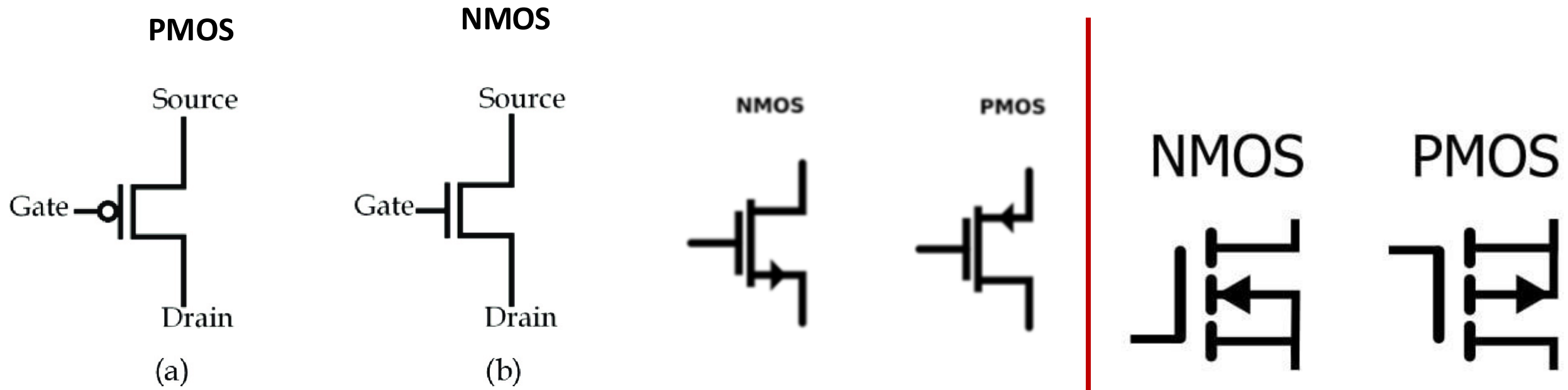


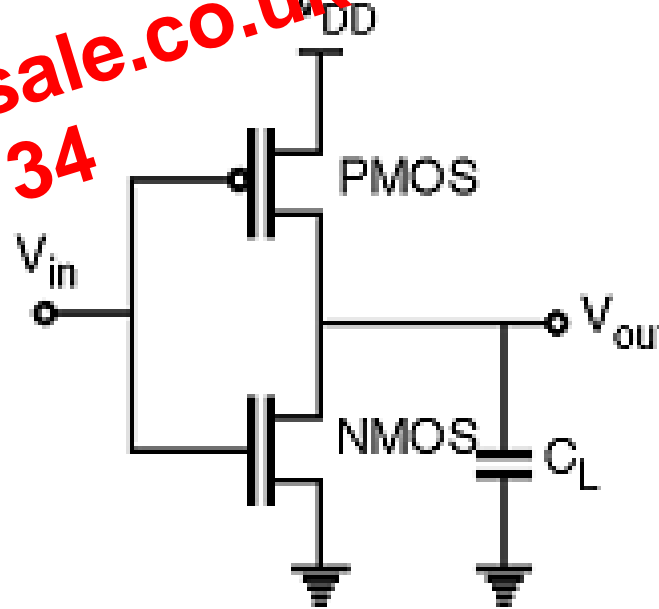
- ❑ MOS structure forms a capacitor, with gate and substrate are as two plates and oxide layer as the dielectric material.
- ❑ The thickness of dielectric material (SiO_2) is usually between 10 nm and 50 nm.
- ❑ It is a majority carrier device, where the current within a conducting channel in between the source & the drain is modulated by an applied voltage to the gate.
- ❑ MOS transistors are classified into two types PMOS & NMOS.



- ❑ The gate-to-source voltage that results in channel inversion is the threshold voltage V_{TH} .
- ❑ This is why NMOS require positive voltages (to attract electrons) and PMOS require negative voltages (to attract holes) for channel formation.
- ❑ The channel presents ohmic resistance for a fixed V_{GS} (linear operation mode) as long as V_{DS} remains smaller than the $V_{GS} - V_{TH}$.
- ❑ After that, the charge concentration near the drain is nulled, and the channel becomes “pinched”.
- ❑ This is called *channel pinch-off*, and marks the division between the saturation and linear regions.
- ❑ As V_{DS} increases, the pinch point moves and the effective length of the channel reduces, which results in the ***channel-length modulation*** effect.

CMOS Inverter Schematic Diagram

Once the input voltage of CMOS changes between 0 to 5 volts, then both the transistors state will be changed accordingly.



The general CMOS inverter structure is the combination of both the PMOS & NMOS transistors where the pMOS is arranged at the top & nMOS is arranged at the bottom. The NMOS transistor is connected at the drain (D) & gate (G) terminals, a voltage supply (VDD) is connected at the source terminal of PMOS & a GND terminal is connected at the source terminal of NMOS. Input voltage (V_{in}) is connected to both the gate terminals of transistors & output voltage (V_{out}) is connected to the drain (D) terminals of the transistor.

DC Transfer Characteristics of CMOS Inverter

CMOS Inverter Voltage Transfer Characteristics

The diagram shows a CMOS inverter circuit. The PMOS transistor has its gate connected to the input V_{in} and its source to V_{DD} . The NMOS transistor has its gate connected to the input V_{in} and its source to V_{SS} . The output V_{out} is taken from the common drain node. Various voltages are labeled: V_{gs} (gate-source voltage), V_{ds} (drain-source voltage), V_{ks} (knee voltage), and V_{dsp} (drain-source voltage of PMOS).

- $V_{Tn} (+V_e)$
- $V_{Tp} (-V_e)$
- $V_{ksn} = (V_k - V_s)_n = V_{in}$
- $V_{psn} = (V_D - V_S)_n = V_{out}$
- $V_{ksp} = (V_k - V_s)_p = V_{in} - V_{DD}$
- $V_{dsp} = (V_D - V_S)_p = V_{out} - V_{DD}$

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Page 21 of 34

The DC input – output transfer characteristic is also called as Voltage Transfer Characteristics (VTC).

It is simply a plot of the output voltage as a function of the input voltage.

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 Page 22 of 34

I - V CHARACTERISTICS OF NMOS

