

1.0.2) **Kirchoff's Voltage Law (KVL)**

Kirchoff's voltage law states that at any instant of time the sum of voltages in a closed circuit equals to zero. KVL may be expressed mathematically as:-

$$\sum_{j=1}^n v_j = 0$$

Where v_j represents the individual voltage in the j th element around the closed circuit having n elements.

If the voltage drop from the positive polarity to the negative polarity is assigned as positive sign, then the voltage rise from the negative polarity to the positive polarity is assumed as negative, or vice-versa.

KVL is a consequence of the fact that no energy is lost or created in an electric circuit. It is our choice whether to apply KVL clock-wise or anti clock-wise. As we go round the loop, it is also our choice to add the voltage drops (and subtract voltage rise) or add the voltage rise (and subtracts voltage drop). Both methods are correct.

However, usually going clock-wise is chosen and voltage drop in elements is set as negative values; meaning that any voltage drop in the closed circuit is subtracted.

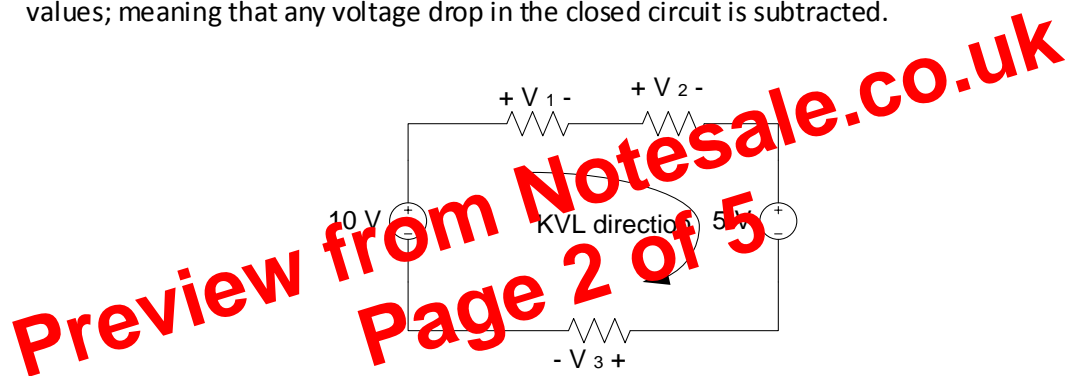


Figure 2 Application of KVL

By applying KVL onto the closed loop in Fig. 2, the equation below is obtained:-

$$10V - V_1 - V_2 - 5V - V_3 = 0$$

By rearranging the equation, the equation for the closed circuit can be rewritten as:-

$$5V = V_1 + V_2 + V_3$$

With KVL, it is obvious that elements in parallel connection have the same voltage drop across them.