

- Q.54** In a bistable multivibrator circuit, commutating capacitor is used
- (A) to increase the base storage charge
 - (B) to provide ac coupling
 - (C) to increase the speed of response
 - (D) to provide the speed of oscillations

Ans. (C)

The commutating capacitor is used for the speedy transition of the state of the bistable.

- Q.55** n-type silicon is obtained by
- (A) Doping with tetravalent element
 - (B) Doping with pentavalent element
 - (C) Doping with trivalent element
 - (D) Doping with a mixture of trivalent and tetravalent element

Ans: (B)

The pentavalent atom provides an excess electron while the other four form the covalent bond with the neighbouring atoms. This excess free electron provides the n type conductivity.

- Q.56** The forward characteristic of a diode has a slope of approximately 50mA/V at a desired point. The approximate incremental resistance of the diode is
- (A) 50Ω
 - (B) 5Ω
 - (C) 20Ω
 - (D) 10Ω

Ans: (C)

Resistance at any point in the forward characteristics is given by $R = \Delta V / \Delta I = 1/50\text{mA} = 20\Omega$

- Q.57** Two stages of BJT amplifiers are cascaded by RC coupling. The voltage gain of the first stage is 10 and that of the second stage is 20. The overall gain of the coupled amplifier is
- (A) 10x20
 - (B) 10+20
 - (C) $(10+20)^2$
 - (D) $(10 \times 20)/2$

Ans: (A)

The voltage gain of a multistage amplifier is equal to the product of the gains of the individual stages.

- Q.58** In the voltage range, $V_p < V_{DS} < BV_{DSS}$ of an ideal JFET or MOSFET
- (A) The drain current varies linearly with V_{DS} .
 - (B) The drain current is constant.
 - (C) The drain current varies nonlinearly with V_{DS} .
 - (D) The drain current is cut off.

Ans: (B)

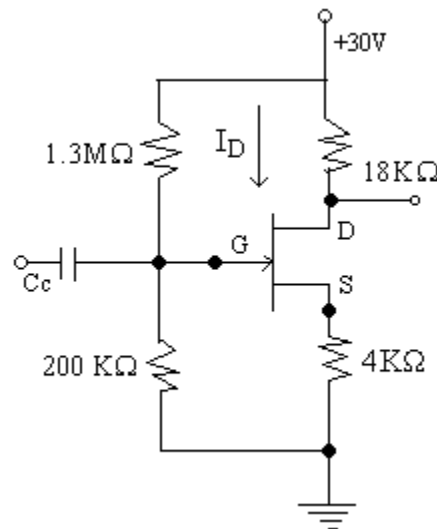
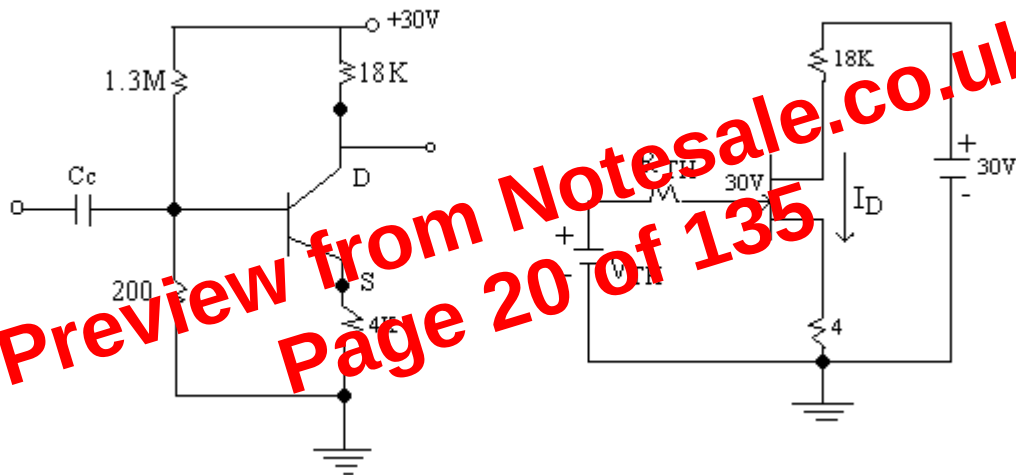


Fig.1

Ans:



The potential divider bias circuit can be replaced by Thevenin equivalent as shown, where

$$R_{TH} = 200K \parallel 1.3M = \frac{200 \times 1300}{200 + 1300} = 173.5K$$

$$V_{TH} = \frac{200K}{1500K} (30) = 4V$$

Applying Kirchhoff's Voltage law to gate-source circuit gives $V_{GS} = V_{TH} - 4I_D$ as there is no gate current flow.

$$\text{Hence } I_D = \frac{V_{TH} - V_{GS}}{4} = \frac{4 - V_{GS}}{4} = I_{DSS} \left(\frac{1 - V_{GS}}{V_P} \right)^2$$

Given, $I_{DSS} = 4 \text{ mA}$ and $V_P = 4 \text{ V}$. substituting these values in the equation for I_P

$$I_D = 4 \left(\frac{1 - V_{GS}}{4} \right)^2$$

Forming the quadratic equation in V_{GS} .

$$V_{BB} = V_{BEQ} + I_{BQ}R_B = V_{BEQ} + \frac{I_{CQ}}{\beta} R_B$$

$$\text{i.e. } V_{BB} = 0.7 + \frac{100 \times 10^{-3}}{40} R_B = 0.7 + 0.0025(2 - 2k) \quad \dots\dots(3)$$

Any value of R_B by which $V_{BB} \leq V_{CC}$ is acceptable. Hence, choosing a reasonable value of 2.2K for R_B , $V_{BB} = 0.7 + 0.0025(2.2 \times 10^3) = 6.2$ volts.

Use equations (1) and (2) to find R_1 and R_2

From (1) $R_B(R_1 + R_2) = R_1R_2$ or $R_1R_2 - R_BR_1 - R_BR_2 = 0$

$$\text{i.e. } R_1(R_2 - R_B) - R_BR_2 = 0, \text{ or } R_1 = \frac{R_BR_2}{R_2 - R_B} \quad \dots\dots(4)$$

substituting the value of R_1 in equation (2)

$$V_{BB} = \frac{R_2}{\left(\frac{R_BR_2}{R_2 - R_B}\right) + R_2} V_{CC} \text{ i.e. } V_{BB} = \frac{(R_2 - R_B)R_2V_{CC}}{R_BR_2 + (R_2)^2 - R_BR_2} = \frac{(R_2 - R_B)}{R_2} V_{CC} \quad \dots(5)$$

$$\text{simplifying, } R_2 = \frac{R_B V_{CC}}{(V_{CC} - V_{BB})} \quad \dots\dots(6)$$

From (4) and (6), we get

$$R_1 = \frac{R_B \frac{R_B V_{CC}}{(V_{CC} - V_{BB})}}{\frac{R_B V_{CC}}{(V_{CC} - V_{BB})} - R_B} = \frac{(R_2)^2 V_{CC}}{R_B V_{CC} - V_{CC} R_B + R_B V_{BB}} = \frac{V_{CC} R_B}{V_{BB}} \quad \dots\dots(7)$$

$$\text{using equation (6), } R_2 = \frac{2.2 \times 12}{12 - 6.2} = 4.55k$$

$$\text{using equation (7), } R_1 = \frac{12 \times 2.2}{6.2} = 4.23k$$

The load R_{ac} at the collector leg of the transistor is reflected load of R_L as per the turns ratio (a) of the transformer.

$$\text{i.e. } R_{ac} = a^2 R_L = \left(\frac{1}{6}\right)^2 (2.5k) = 69.4\Omega$$

As i_c swings ± 80 mA either side of $I_{CQ} = 100$ mA on the R_{ac} load line, and $V_{CEQ} = 12V$ (DC load line being almost vertical)

$$\begin{aligned} V_{CE\max} &= V_{CEQ} + I_{Cm}R_{ac} = 12 + 80 \times 10^{-3} \times 69.4 \\ &= 12 + 5.55 = 17.55 \text{ Volts.} \end{aligned}$$

Hence, Maximum Load voltage_(secondary):

$$V_{L\max} = \frac{1}{a} I_{cm} R_{ac} = 6 \times (80 \times 10^{-3}) (69.4) = 33.31V$$

Hence, Maximum Load current:

$$I_{L\max} = a I_{cm} = \frac{1}{6} (80 \times 10^{-3}) = 13.33mA.$$

- Q.9** A negative feedback of $\beta = 2.5 \times 10^{-3}$ is applied to an amplifier of open loop gain 1000. Calculate the change in overall gain of the feedback amplifier if the gain of the internal amplifier is reduce by 20%. (4)

Ans:

If A is the gain of the basic amplifier, the overall gain A_f of the amplifier with negative f.b. is

$$A_f = \frac{A}{1 + A\beta} \text{ given } A = 1000 \text{ and } \beta = 2.5 \times 10^{-3},$$

$$A_f = \frac{1000}{1 + 1000 \times 2.5 \times 10^{-3}} = \frac{1000}{1 + 2.5} = 285.7$$

When A is reduced by 20%, the new A, say $A_n = 1000 - 0.2 \times 10^3 = 800$

The new voltage gain with f.b. is

$$A_f = \frac{800}{1 + 800 \times 2.5 \times 10^{-3}} = 266.67.$$

- Q.10** A full wave rectifier is fed with a voltage, $50 \sin 100 \pi t$. Its load resistance is 400Ω . The diodes used in the rectifier have an average forward resistance of 30Ω . Compute the (i) average and rms values of load current, (ii) ripple factor and (iii) efficiency of rectification. (6)

Ans:

The maximum value of load current

$$I_{L \max} = \frac{V_{\max}}{R_L + R_F}; \text{ given } V_{\max} = 50 \text{ volts; } R_L = 400 \Omega, R_F = 30 \Omega$$

$$\text{Thus } I_{L \max} = \frac{50}{400 + 30} = 0.1163 \text{ Amp}$$

$$\text{Average current } I_{\text{avg}} = \frac{2 I_{\max}}{\pi} \text{ for a FWR}$$

$$\text{i.e. } I_{\text{avg}} = \frac{2 \times 0.1163}{\pi} = 0.074 \text{ A or } 74 \text{ mA} = I_{\text{dc}}$$

The r.m.s value of load current is

$$I_{\max} = \frac{I_{\max}}{\sqrt{2}} = \frac{0.1163}{\sqrt{2}} = 0.0822 \text{ A or } 82.2 \text{ mA}$$

$$\text{Ripple factor } \gamma = \sqrt{\left(\frac{I_{\text{rms}}}{I_{\text{dc}}}\right)^2 - 1} = \sqrt{\frac{(0.0822)^2}{(0.074)^2} - 1} = 0.483$$

Efficiency of rectification in a FWR is given by

$$= AB + \overline{AB}(C + \overline{C}) + \overline{B}CA + \overline{A}\overline{B}C$$

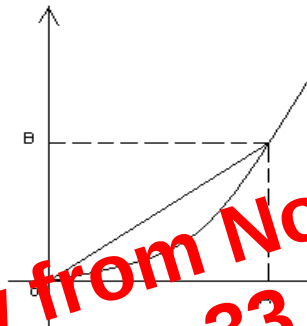
$$= ABC + \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{B}CA + \overline{A}\overline{B}C$$

		BC			
A	0	00	01	11	10
	0	1	1	1	1
	1		1		

- Q.25** A load line intersects the forward V-I characteristic of a silicon diode at Q, where the slope of the curve is 40mA/V. Calculate the diode resistance at the point Q. (4)

Ans:

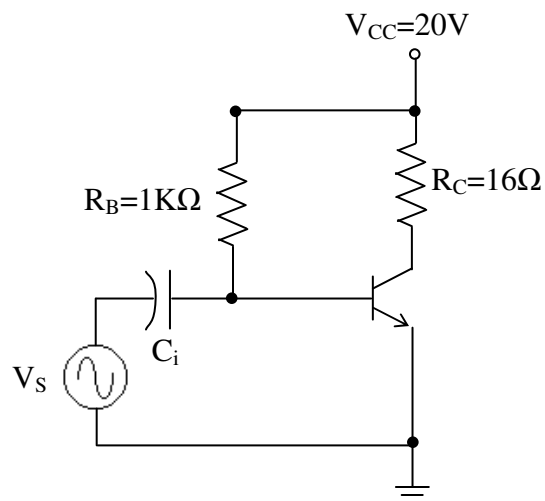
DC or static resistance, $R = \frac{V}{I} = \frac{OA}{OB}$



$$R = \frac{V}{I} = \frac{1}{40 \text{ mA/V}}$$

$$R = 25 \Omega$$

- Q.26** The power amplifier shown below is operated in class A, with a base current drive of 8.5mA peak. Calculate the input dc power, the power dissipated in the transistor, the signal power delivered to the load and the overall efficiency of the amplifier, if transistor $\beta=30$ and $V_{BE}=0.7\text{V}$. (8)



Ans:

$$I_{c(Sat)} = \frac{V_{cc}}{R_c} = \frac{20}{16} = 1.25A$$

$$V_{cE} = V_{cc} = 20v$$

Now dc – load line is drawn joining points (20v, 0) and (0, 1.25A)

For operating point Q,

$$I_B = \frac{V_{cc} - V_{BE}}{R_B} = \frac{20 - 0.7}{1k} = 19.3mA$$

$$I_{cQ} = \beta I_B = 30 \times 19.3mA = 0.579A$$

$$V_{cEQ} = V_{cc} - I_{cQ} R_c = 20 - 0.579 \times 16 = 10.736v$$

$$I_{c_{peak}} = \beta I_{b_{peak}} = 30 \times 8.5mA = 0.255A$$

$$P_{in(dc)} = V_{cc} I_{cQ} = 20 \times 0.579 = 11.58w.$$

$$P_{out(ac)} = \left(\frac{I_{c_{peak}}}{\sqrt{2}} \right)^2 R_c = \left(\frac{0.255}{\sqrt{2}} \right)^2 \times 16$$

$$= 0.5202 w.$$

Power delivered to the transistor,

$$P_{tr(dc)} = V_{cc} I_{cQ} - I_{cQ}^2 R_c$$

$$= 20(0.579) - (0.579)^2 \cdot 16$$

$$= 6.216w$$

$$\text{Power lost in transistor} = P_{tr(dc)} - P_{out(ac)}$$

$$= 6.216 - 0.5202$$

$$= 5.6958$$

$$\text{Collector Efficiency, } \eta_{colleff} = \frac{P_{out(ac)}}{P_{tr(dc)}} \times 100$$

$$= \frac{0.5202}{6.216} \times 100$$

$$= 8.368 \%$$

Power rating of transistor = Zero-signal power dissipation

$$= V_{cEQ} I_{cQ}$$

$$= 10.736 \times 0.579$$

$$= 6.216w.$$

Q.27 Find the period of the output pulse in the circuit shown below:

(4)

$$\begin{aligned}
 &= I_{rms}^2 R_F + I_{rms}^2 R_L = I_{rms}^2 (R_F + R_L) \\
 &= \frac{I_{max}^2}{4} (R_F + R_L) \\
 \eta &= \frac{P_{dc}}{P_{ac}} = \frac{I_{max}^2 \frac{R_L}{\pi^2}}{I_{max}^2 (R_F + R_L) / 4} = \frac{4}{\pi^2} \frac{R_L}{R_F + R_L} \\
 \eta &= \frac{0.406}{1 + R_F/R_L} \quad \text{i.e. 40.6 \% if } R_F \text{ is neglected.}
 \end{aligned}$$

Full-wave rectifier:

$$\begin{aligned}
 P_{dc} &= I_{dc}^2 R_L = \left(\frac{2}{\pi} I_{max} \right)^2 R_L = \frac{4}{\pi^2} I_{max}^2 R_L \\
 P_{ac} &= I_{rms}^2 (R_L + R_F) = \frac{I_{max}^2}{2} (R_L + R_F) \\
 \text{Rectification efficiency, } \eta &= \frac{P_{dc}}{P_{ac}} = \frac{\frac{4}{\pi^2} I_{max}^2 R_L}{\frac{I_{max}^2}{2} (R_L + R_F)} \\
 \eta &= \frac{8}{\pi^2} \frac{1}{1 + R_F/R_L} = \frac{0.812}{1 + R_F/R_L} \\
 \eta &= 81.2 \% \quad \text{if } R_F \text{ is neglected.}
 \end{aligned}$$

- Q.29** An intrinsic silicon bar is 4mm long and has a rectangular cross section $60 \times 100 (\mu\text{m})^2$. At 300K, find the electric field intensity in the bar and voltage across the bar when a steady state current of 1μA is measured. (Resistivity of intrinsic silicon at 300K is $2.3 \times 10^3 \Omega\text{-m}$) (7)

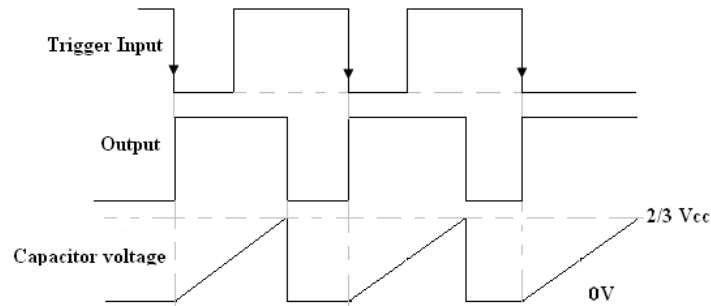
Ans:

$$\begin{aligned}
 \text{Length} &= 4\text{mm} \\
 A &= 60 \times 100 (\mu\text{m})^2 \\
 \text{Current } I &= 1\mu\text{A} \\
 \text{Resistivity } r &= 2.3 \times 10^3 \Omega\text{m} \\
 J &= \sigma E \\
 E &= J / \sigma = (I/A) (1/\sigma) = (I/A) r \\
 E &= (1 \times 10^{-6} / (60 \times 10^{-6} \times 100 \times 10^{-6})) \times 2.3 \times 10^3 \\
 &= 383.33 \times 10^3 \text{ V/m} \\
 V &= EL = 383.33 \times 10^3 \times 4\text{mm} = 1.53 \times 10^3 \text{ V}
 \end{aligned}$$

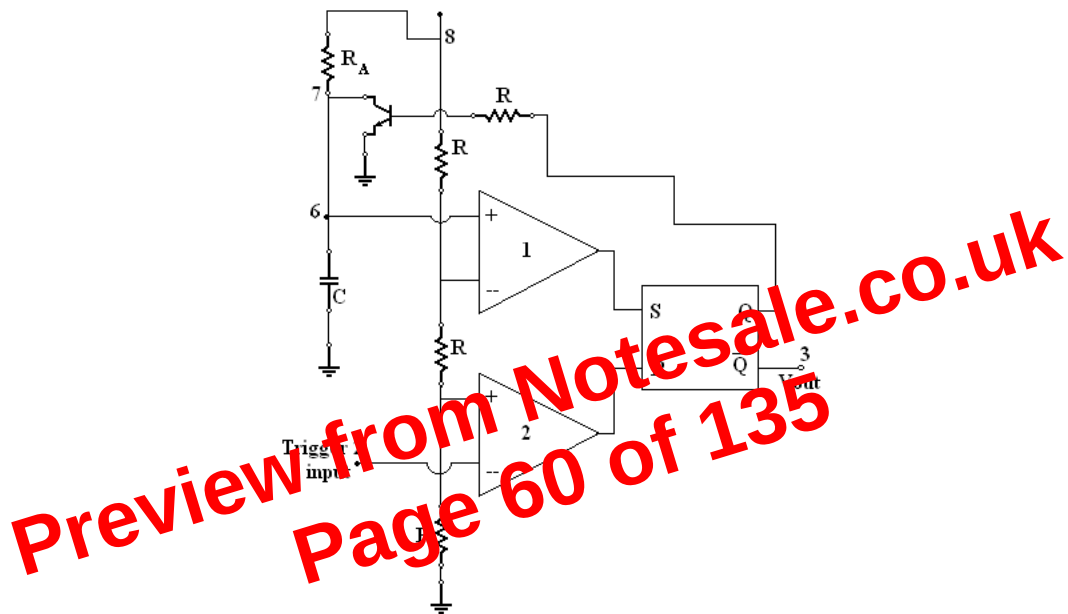
- Q.30** The resistivity of doped silicon material is $9 \times 10^{-3} \text{ ohm-m}$. The Hall co-efficient is $3.6 \times 10^{-4} \text{ m}^3 \text{ coulomb}^{-1}$. Assuming single carrier conduction, find the mobility and density of charge carrier ($e = 1.6 \times 10^{-19} \text{ coulomb}$) (7)

Ans:

$$\begin{aligned}
 R_H &= 3.6 \times 10^{-4} \text{ m}^3 / \text{coulomb}, \rho = 9 \times 10^{-3} \text{ ohm-m} \\
 \text{Mobility} = \mu_n &= \sigma R_H = (1/\rho) R_H = (1/9 \times 10^{-3}) \times 3.6 \times 10^{-4} = 400 \text{ cm}^2 / \text{V-s} \\
 \text{Density of charge carriers} &= \sigma \mu
 \end{aligned}$$



Trigger Input, Output and Capacitor Voltage Wave Forms

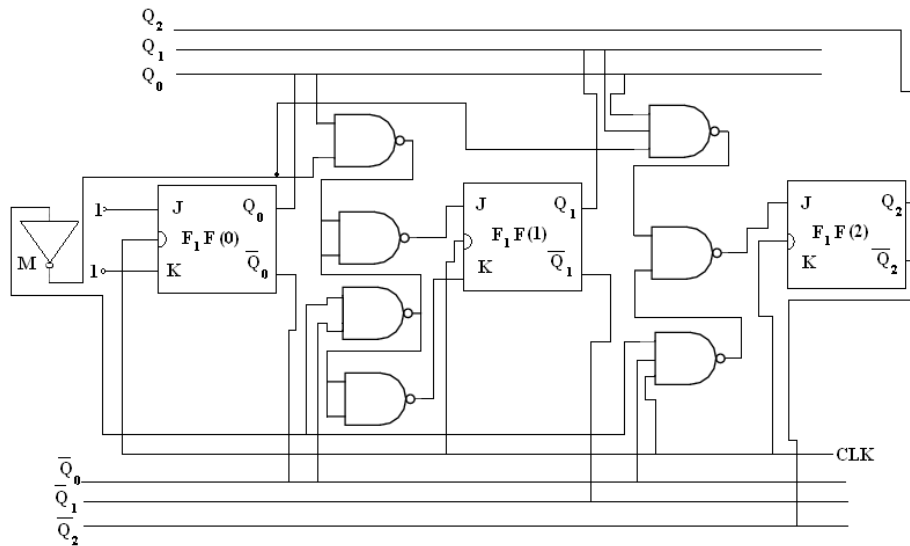


Internal Circuitry with external connections

Operation:

Initially, when the output at pin-3 is low i.e., the circuit is in a stable state, the transistor is on and capacitor C is shorted to ground, when a negative pulse is applied to pin 2, the trigger input false below $\frac{1}{3}V_{cc}$, the output of comparator goes high which resets the flip-flop and consequently the transistor turns off and output at pin-3 goes high. As the discharge transistor is cut-off, the capacitor C begins charging towards $+V_{cc}$ through resistance R_A with a time constant equal to $R_A C$. When the increasing capacitor voltage becomes slightly greater than $+\frac{2}{3}V_{cc}$, the output of comparator-1 goes high, which sets the flip-flop. The transistor goes to saturation, thereby discharging the capacitor C and output of the timer goes low.

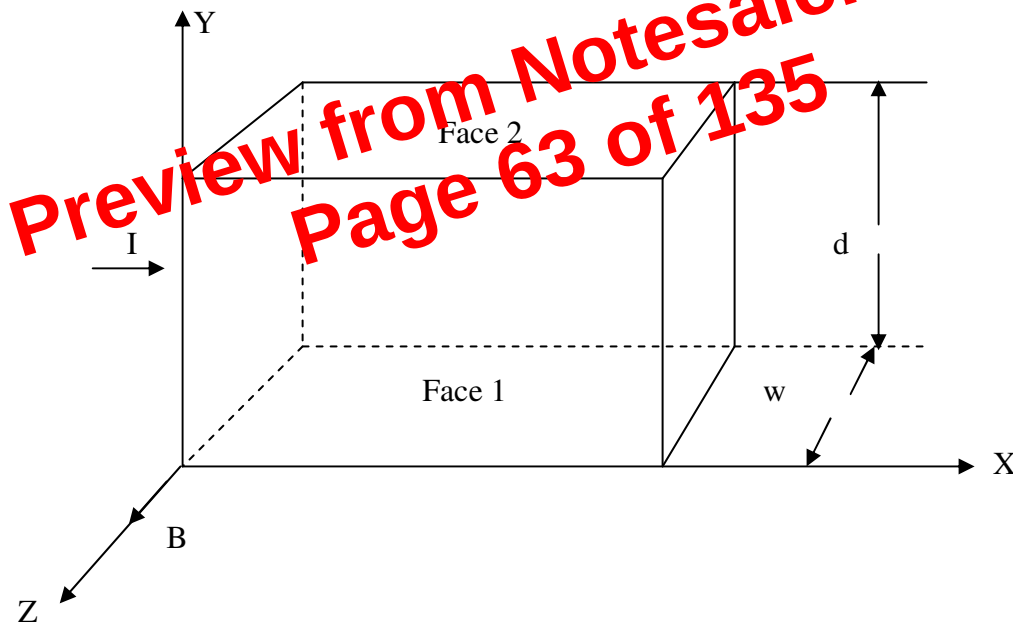
- Q.16** Write the circuit diagram of a square wave generator using an opamp and explain its operation. (7)



Logic diagram of 3 bit UP – DOWN Counter

Q.18 Describe how conductivity and carrier mobility of a sample of semiconductor can be determined by subjecting it to Hall-effect. (8)

Ans:



When a specimen (Metal or Semiconductor) is placed in a transverse magnetic field and a direct current is passed through it, then an electric field is induced across its edges in the perpendicular direction of current as well as magnetic field. Thus phenomenon is called the **Hall-Effect**.

A semiconductor bar carrying a current I in the positive X -direction and placed in a magnetic field B acting in the positive Z -direction.

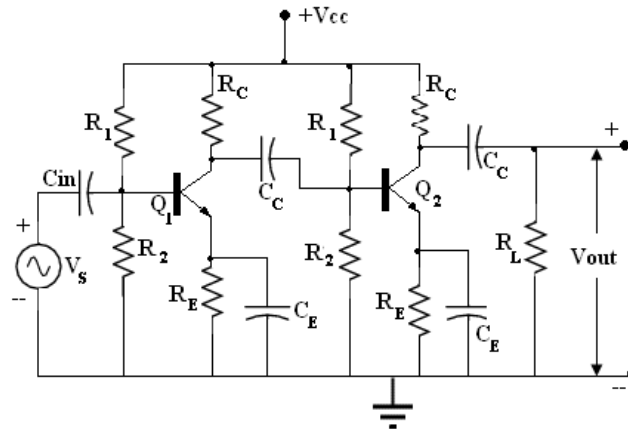
In the equilibrium state the electric field intensity E due to Hall-effect must exert a force on the charge carriers which just balances the magnetic force.

$$\text{i.e. } eE = Bev$$

equal to $-V - (V - V_o)$ or $-(2V - V_o)$. Thus peak-to-peak output being the difference of the negative and positive peak voltage levels is equal to $V_o - [-(2V - V_o)]$ or $2V$.

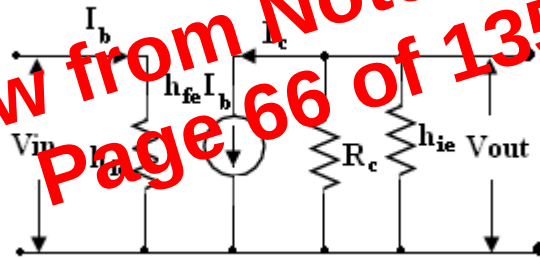
- Q.21** Draw the circuit of a RC-coupled amplifier. Explain its behaviour at low, mid and high frequencies by drawing separate equivalent circuit for each frequency region. **(16)**

Ans:



Two stage RC- Coupled Transistor Amplifier

1. Mid Frequency Range

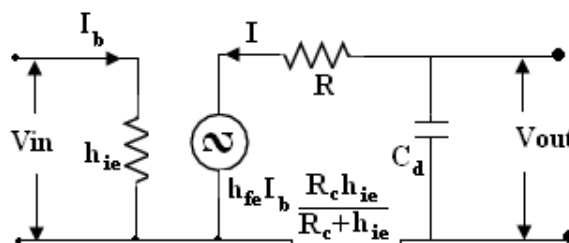


$$\text{Current, } I = \frac{h_{fe} I_b R_c}{R_c + h_{ie}}$$

$$\text{So current gain, } A_{in} = \frac{I}{I_b} = \frac{h_{fe} I_b R_c}{R_c + h_{ie}}$$

$$V_{out} = h_{ie} I = \frac{h_{ie} h_{fe} I_b R_c}{R_c + h_{ie}}$$

2. High Frequency Range



Thevenin's equivalent circuit

Q.26 Prepare the truth-table for the function

$$f(a, b, c) = \bar{a}bc + a\bar{b}c + ab\bar{c}$$

Minimize the function using K-map. Draw the logic diagram using gates of your choice to realize the minimized function. (8)

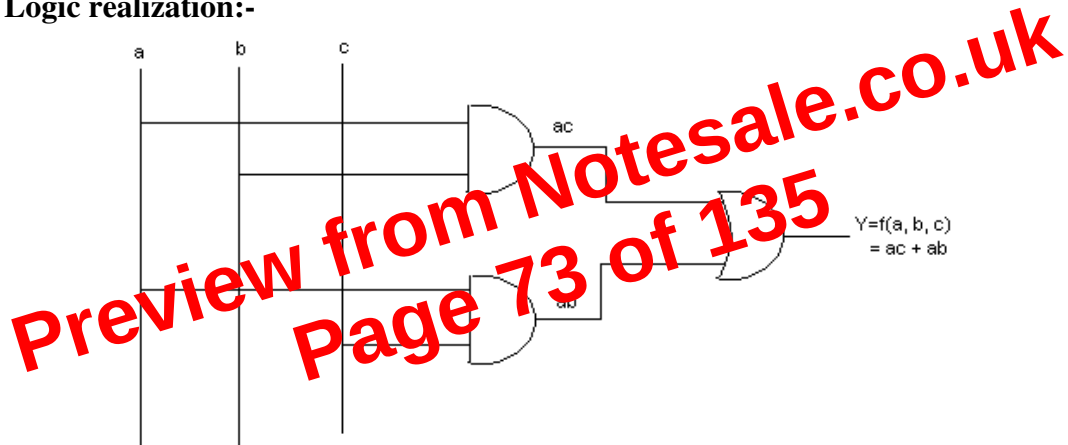
Ans:

The function is $f(a, b, c) = \bar{a}bc + a\bar{b}c + ab\bar{c}$

		bc			
		a	00	01	11
	0				
	1			1	1

$$f(a, b, c) = ac + ab$$

Logic realization:-



Q.27 Define mobility in a semiconductor. Does it also depend on doping levels? (3)

Ans:

In the presence of electric field in a semiconductor, the electrons move with an average velocity called drift velocity. Mobility is the ratio of drift velocity and electric field.

The drift velocity is given by $v_d = \mu E$ where

E = Electric field

μ = constant called “mobility” of the charge carrier.

Yes, the mobility depends on the doping levels.

Q.28 What is the quantity of mobility for electrons and for holes in a silicon semiconductor? (2)

Ans:

The typical value of mobility of electrons in a silicon semiconductor is $0.13 \text{ m}^2/\text{V-s}$ and that of holes is $0.046 \text{ m}^2/\text{V-s}$.

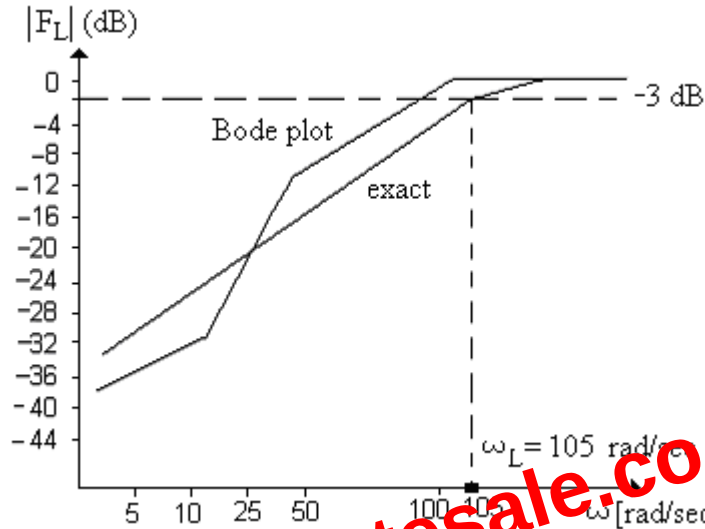
In many cases zeros have lower frequency much smaller than ω_L . Also one of the poles will have much higher frequency than all the other poles.

Therefore $F_L(s) \cong s / (s + \omega_{p1})$, where ω_{p1} = the largest value pole.

In this case, low frequency response of amplifier is dominated by the pole at

$s = -\omega_{p1}$ and lower 3dB frequency is approximately $= \omega_{p1}$

i.e., $\omega_L \approx \omega_{p1}$



This is called as dominant pole approximation. This approximation can be made if highest frequency pole is separated from nearest pole or zero by a least 2 octaves (i.e., factor of 4). If dominant low frequency pole does not exist then

$$\omega_L = \sqrt{\omega_{p1}^2 + \omega_{p2}^2 - 2\omega_{p1}\omega_{p2}}$$

If $F_L(s) = (s(s+10)) / ((s+100)(s+25))$

$\omega_{p1} = 100 \text{ rad/sec}$ is 2 octaves higher than 2^{nd} pole and a decade higher than 0.

Hence, $\omega_L = \omega_{p1} = 100 \text{ rad/sec}$

$$\text{Or } \omega_L = (\omega_{p1}^2 + \omega_{p2}^2 - 2\omega_{p1}\omega_{p2})^{1/2}$$

$$\omega_L = \sqrt{\omega_{p1}^2 + \omega_{p2}^2 - 2\omega_{p1}\omega_{p2}}$$

$$= \sqrt{(100^2 + 25^2 - 2 \times 10^2)} = 102 \text{ rad/sec}$$

- Q.34** Draw the characteristics of an n channel JFET. Enunciate the linear relationship that represents the i_p - V_s characteristics near the origin. (8)

Ans:

The figure below shows a family of I_D v/s V_{DS} characteristics of an n channel JFET for various values of V_{GS} . For small values of V_{DS} (below pinch-off), the depletion region of the gate would not be affected much by the flow of drain current I_D from one end of the gate to the other end of the gate. This is true for a given value of V_{GS} . As such, a linear relationship exists between I_D and V_{DS} and the JFET behaves like a voltage-controlled resistor.

An enhancement n-channel MOSFET is biased with a battery V_{GS} . A time varying signal v_{gs} which is to be amplified is superimposed on gate to source dc bias V_{GS} . Thus the total instantaneous gate voltage is

$$v_{GS} = V_{GS} + v_{gs}$$

The operating point can be got by intersection of load line and I_D versus V_{DS} curve corresponding to instantaneous values of v_{GS} .

When a sinusoidal signal v_{GS} is applied the instantaneous operating point will move along the load line in correspondence with total instantaneous voltage v_{GS} . The output signal is an amplified replica of the input signal. Linear amplification can be obtained by properly choosing the dc bias point Q and by keeping the input signal amplified.

FET as voltage dependent resistor:

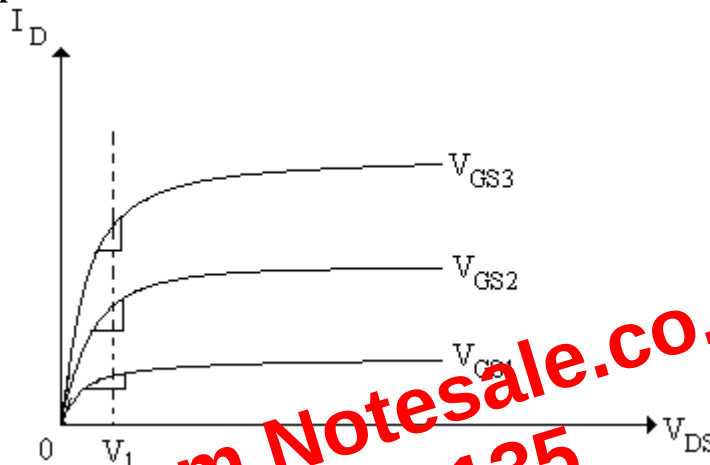


FIG: 9 (ii)

Figure 9 (ii) shows the output characteristics of an FET. It shows the variations of I_D with V_{DS} for constant V_{GS} .

If we consider the slope of the curve for low values of V_{DS} , we see that the slope varies with variations in V_{GS} . As the slope is related to the resistance, we can say that the resistance would be different for different values of V_{GS} .

Hence for a given $V_{DS} = V_1$, the resistance depends on gate voltage and thus it is seen that FET acts as voltage dependent resistor.

- Q.43** What is a tuned amplifier? What is the fundamental difference between audio amplifiers and tuned amplifiers? How is bandwidth related to resonant frequency (f_r) and the quality factor (Q). (7)

Ans:

Tuned amplifiers are the ones, which amplify a specific frequency or a narrow band of frequencies. Audio amplifiers provide the constant gain over a wide band of frequencies. Tuned amplifiers are designed to have specific, usually narrow bandwidth. This is shown in **Fig. 10 (a)**. BW_A is the bandwidth of response of a typical audio amplifier, while BW_T is the bandwidth of tuned amplifier and f_r is called the center frequency of tuned amplifier.

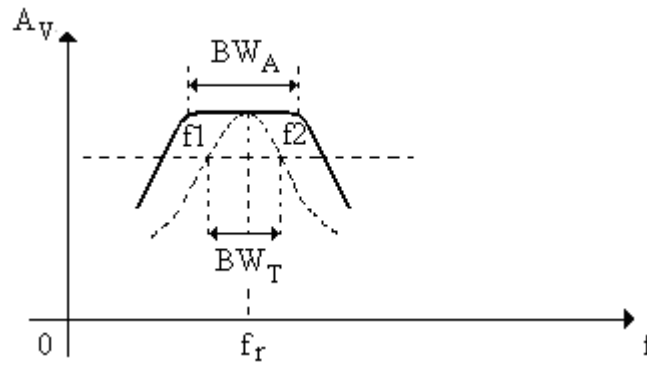


Fig. 10(a)

The quality factor Q of a tuned amplifier is equal to the ratio of center frequency (f_r) to bandwidth (BW_T) i.e

$$Q = f_r / BW_T$$

Q is determined by the circuit component values. For a parallel resonance circuit is given by $f_r = 1 / (2\pi\sqrt{LC})$ and $Q = X_L / R$ where X_L is the reactance of the inductor having resistance R .

Q.44 Discuss the terminal properties of an ideal operational amplifier.

Ans:

The **Fig. 11(a)** shows the schematic of an ideal op-amp. The following are the important properties of an ideal op-amp.

- The input impedance of an ideal op-amp is infinite. Hence it draws no current at both the input terminals.
- The gain of an ideal op-amp is infinite (∞), hence the differential input $V_d = V_1 - V_2$ is zero for the finite output voltage V_o .

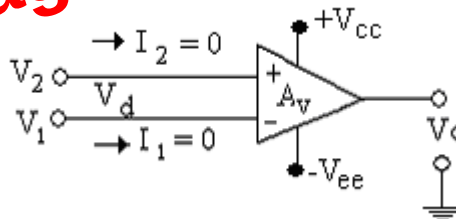


Fig. 11(a)

- The output voltage V_o is independent of the current drawn from the output terminal. Thus its output impedance is zero.

This results in the following Characteristic of an ideal op-amp.

- Infinite Voltage gain:** It is denoted as A_{OL} . It is the differential open loop gain.
- Infinite input impedance:** It is denoted as R_{in} and ensures that no current flows into an ideal op-amp.
- Zero output impedance:** It is denoted as R_o and ensures that the output voltage of the op-amp remains the same, irrespective of the load.
- Zero offset voltage:** This ensures zero output for zero input signal voltage in an ideal op-amp.
- Infinite bandwidth:** This ensures that the gain of the op-amp will be constant over the frequency range from d.c to infinite.

The equivalent circuit of the amplifier is shown in Fig.16a(ii),

$$R_t = R_o \parallel R_p \parallel R_i$$

where R_o = output resistance of current generator $g_m V_{be}$ and is equal to $(1/h_{oe})$

R_i = input resistance of next stage

R_p = equivalent internal resistance of L calculated when series L circuit is represented by its equivalent parallel circuit.

$$\text{Voltage Gain } A_V = V_o/V_i$$

From Fig.16a(iii) output voltage can be given as

$$V_o = -g_m V_{be} Z$$

where Z = impedance of C, L and R_t in parallel or,

$$Z = R_t / (1 + 2jQ_{eff}\delta)$$

$$Q_{eff} = R_t / \omega_r L$$

and ω_r = resonant frequency

and δ = fractional variation in resonant frequency = $(\omega - \omega_r) / \omega_r$

At resonant frequency $\omega = \omega_r$ and $\delta = 0$.

$$Z \text{ (at resonance)} = R_t$$

Fig.16a(iii) shows the final equivalent circuit of Fig.16a(ii).

Hence $V_o = -g_m V_{be} R_t$ at resonance

Also $V_{be} = V_i (r_{be} / (r_{bb} + r_{be}))$ (from Fig.16a(ii) neglecting C_s)

$$V_o = -g_m V_i (r_{be} Z / (r_{bb} + r_{be}))$$

$$A_V = V_o/V_i = -g_m V_i (r_{be} Z / (r_{bb} + r_{be}))$$

$$= -g_m (r_{be} / (r_{bb} + r_{be})) \times (R_t / (1 + 2jQ_{eff}\delta))$$

At resonance, voltage gain is

$$A_V = -g_m (r_{be} / (r_{bb} + r_{be})) \times R_t$$

Q.48 Explain the reasons for potential instability in tuned amplifiers. (7)

Ans:

A tuned amplifier is required to be highly selective. Instability is because of positive feedback in tuned amplifiers.

Q.49 What are 'intrinsic' and 'extrinsic' semiconductors? Comment on the conductivity of extrinsic semiconductor. (4)

Ans:

A pure semiconductor which is not doped is said to be intrinsic semiconductor. They have very low conductivity. When pure semiconductors are mixed (doped) using trivalent or pentavalent elements, we get extrinsic ones, which are p type in the former case and n type in the latter.

The crystalline nature of the original semiconductor is unaltered by doping as the doping element atoms replace the original semiconductor atoms without disturbing the crystal structure as such. This happens by participation of electrons of doping element with those of semiconductor in forming bonds. However, either an extra electron as in the case of pentavalent dopant or a free hole as in the case of trivalent dopant greatly enhances the conductivity.

Q.50 Explain the classification of power amplifiers according to operational modes. (6)

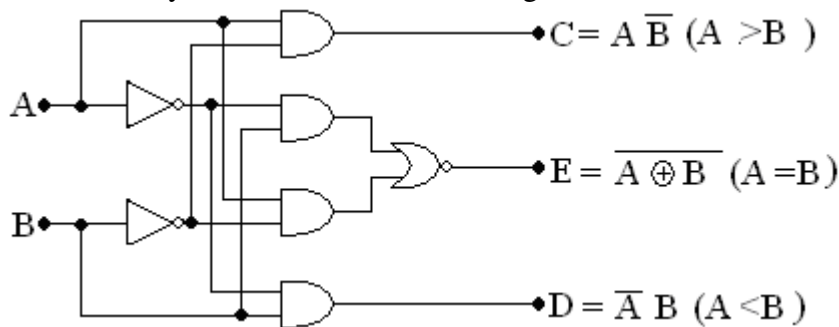
The transfer characteristics i.e., V_{in} v/s V_o is shown in Fig.(iii).

Due to the positive feedback the comparator is said to exhibit hysteresis. The portion without arrows may be traversed in either direction, but other segments can be obtained only if V_2 is increased or decreased in given direction.

Because of hysteresis, circuit triggers at a higher voltage for increasing than for decreasing signals.

iv) The digital comparator:

A comparator is used to detect whether a binary number is greater than, equal to or less than another binary number. Consider two single bit numbers A and B,



One bit comparator

Where $C=1$ for $A>B$

$E=1$ for $A=B$

$D=1$ for $A<B$

a) Let $A=B$

EX - NOR gate is an equality detector. The output E of EX-NOR is given by

$$E = \overline{A}B + A\overline{B} = \begin{cases} 1 & A = B \\ 0 & A \neq B \end{cases}$$

b) Condition $A>B$ is given by $C=\overline{A}B=1$ because if $A>B$ then $A=1$ and $B=0$ therefore $C=1$ here

if $A=B$ or $A<B$ ($A=0$, $B=1$) then $C=0$.

c) Condition $A<B$ is determined from $D=\overline{A}B=1$

Consider a 4-bit comparator. ($\overline{A}$ & $\overline{B}$ are 4 bit numbers).

a) For $A = B$, $A_3 = B_3$, $A_2 = B_2$, $A_1 = B_1$, $A_0 = B_0$

Therefore $E=E_3E_2E_1E_0$

If $A = B$ then $E = 1$

If $A \neq B$ then $E = 0$

b) For $A>B$: $A_3>B_3$ (MSB)

Or $A_3=B_3$ and $A_2>B_2$

Or $A_3=B_3$ and $A_2=B_2$ and $A_1>B_1$

Or $A_3=B_3$ and $A_2=B_2$ and $A_1=B_1$ and $A_0>B_0$

This is given by

$$C = \overline{B}_3A_3 + \overline{B}_2E_3A_2 + \overline{B}_1E_3E_2A_1 + \overline{B}_0E_3E_2E_1A_0$$

If $A>B$ then $C = 1$

d) For $A<B$: in the above equation interchange A and B, to get the output D.

Digital comparators are useful in comparing binary words and the result of comparison is used to initiate various actions in a digital system.

FlipFlop-B changes state on next clock pulse each time $Q_A = 1$ and $Q_D = \overline{1}$ so that

$$J_B = \overline{K_B} = Q_A Q_D.$$

This is implemented by ANDing Q_A and $\overline{Q_D}$ and connecting the gate output to JK inputs of FlipFlop -B.

Clock	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

FlipFlop-C changes on next clock pulse each time both $Q_A = 1$ and $Q_B = 1$

$$J_C = K_C = Q_A Q_B$$

This is implemented by ANDing Q_A and Q_B and connecting gate output to JK inputs of FlipFlop F-C.

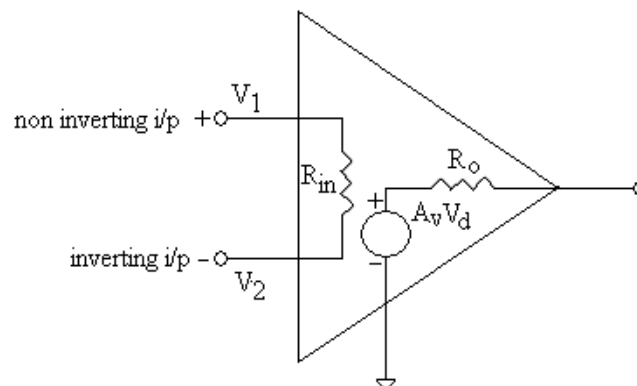
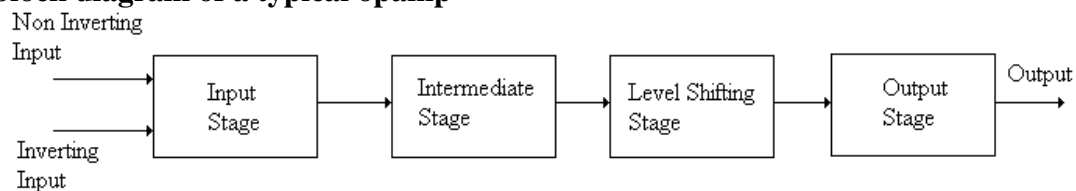
FlipFlop -D changes on next clock pulse each time $Q_A = 1$ and $Q_B = 1$, $Q_C = 1$ or when $Q_A = 1$ and $Q_D = 1$

$$J_D = K_D = Q_A Q_B Q_C + Q_A Q_D$$

- Q.75** Draw the block schematic of a typical operational amplifier and briefly explain the function of each block. Also give the equivalent circuit of the opamp. (9)

Ans:

The block diagram of a typical opamp



Equivalent circuit of the opamp

$$I_{RMS} = \sqrt{\left(\frac{1}{2\pi} \int_0^{2\pi} i_L^2 d\omega t \right)} = \sqrt{\left(\frac{2}{2\pi} \int_0^{\pi} (I_m \sin \omega t)^2 d(\omega t) \right)}$$

$$= I_m \sqrt{\frac{1}{\pi} \int_0^{\pi} [(1 - \cos 2\omega t)/2] d(\omega t)} = I_m / \sqrt{2}$$

In bridge rectifier, in each half cycle two diodes conduct simultaneously. Hence maximum value of load current is

$$I_m = E_m / (R_s + 2R_f + R_L), \text{ where } R_s = \text{transformer secondary winding resistance.}$$

$$P_{DC} = I_{DC}^2 R_L = (2I_m/\pi)^2 R_L$$

$$P_{AC} = I_{rms}^2 (2R_f + R_s + R_L) = (I_m/\sqrt{2})^2 (2R_f + R_s + R_L)$$

$$\text{Therefore, rectification efficiency} = \frac{P_{DC}}{P_{AC}} = \frac{[(4I_m^2/\pi^2) R_L]}{I_m^2/2 (2R_f + R_s + R_L)} \approx \frac{8R_L}{\pi^2 R_L} \quad (\text{since } 2R_f + R_s \ll R_L)$$

$$= 8/\pi^2 = 81.05\%$$

$$\text{Ripple factor} = \sqrt{(I_{rms}/I_{DC})^2 - 1}$$

$$= \sqrt{[(I_m/\sqrt{2}) / (2I_m/\pi)]^2 - 1} = \sqrt{(\pi/\sqrt{2})^2 - 1} = 0.48.$$

The Fig. 39a(iii) shows how a capacitor filter is connected to the rectifier output and the output voltage waveform of the rectifier across the load, with capacitor filter.

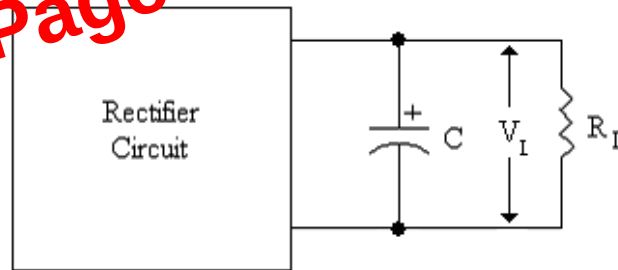


Fig. 39a(iii)

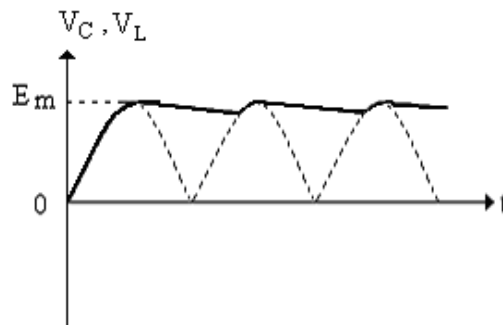
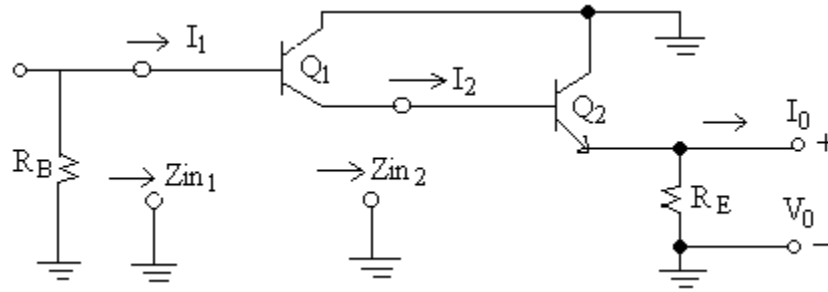


Fig. 39a(iv)

The dotted line in Fig. 39a(iv) shows the rectifier output without filter and solid line shows the output across the capacitor filter.



Considering Q_2 , $Z_{in2} = h_{fe2} R_E$ (1)

Current Gain: $A_{i2} = I_{0e2} / I_2 = I_{e2} / I_{b2} \simeq h_{fe2}$ (2)

For transistor Q_1 , $1/h_{oe1}$ is comparable with becomes the load impedance for Q_1 .

Hence without neglecting $1/h_{oe1}$, the current gain for Q_1 is

$$A_{i1} = \frac{I_2}{I_1} = \frac{h_{fe1}}{1 + h_{oe1} Z_{in2}} = \frac{h_{fe1}}{1 + h_{oe1} (h_{fe2} R_E)} \quad \text{.....(3)}$$

If $h_{fe1} = h_{fe2}$ and $h_{oe1} = h_{oe2} = h_{oe}$, equation (3) can be written as

$$A_{i1} = \frac{h_{fe}}{1 + h_{oe} (h_{fe} R_E)} \text{ and } A_{i2} = h_{fe}$$

The overall gain of the amplifier is $A_i = A_{i1} A_{i2}$

$$\text{i.e., } A_i = \frac{h_{fe}^2}{1 + h_{oe} h_{fe} R_E} \quad \text{.....(4)}$$

For $h_{oe} h_{fe} R_E \ll 1$, a good approximation would be ignored w.r.t Z_{in2} ,(5)

Input Impedance

$$\begin{aligned} Z_{in1} &= h_{fe1} \left(Z_{in2} \parallel \frac{1}{h_{oe1}} \right) = h_{fe1} \left(h_{fe2} R_E \parallel \frac{1}{h_{oe1}} \right) \\ &= \frac{h_{fe1} h_{fe2} R_E}{h_{oe1} h_{fe2} R_E + 1} \end{aligned}$$

If $h_{fe1} = h_{fe2} = h_{fe}$ and $h_{oe1} = h_{oe2} = h_{oe}$ then

$$Z_{in1} = \frac{h_{fe}^2 R_E}{h_{oe} h_{fe} R_E + 1}$$

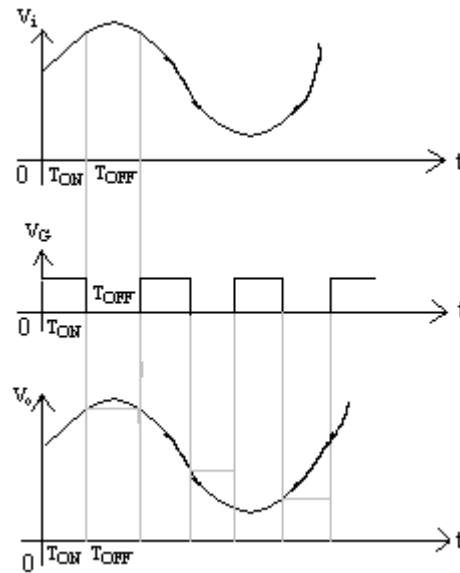
if $h_{oe} h_{fe} R_E \leq 0.1$, then $Z_{in1} \simeq h_{fe}^2 R_E = \beta^2 R_E$

The advantage of darlington amplifier is its very high current gain and very high Z_{in} . It is used to isolate high impedance source from low impedance load.

Q.94 Draw the circuit of common source amplifier using JFET and show its equivalent circuit. Analyse the equivalent circuit to find an expression for voltage gain and output resistance. (6)

Ans:

The circuit of n-channel, JFET common source amplifier is shown below in fig(1) and its ac equivalent circuit is shown in fig(2).



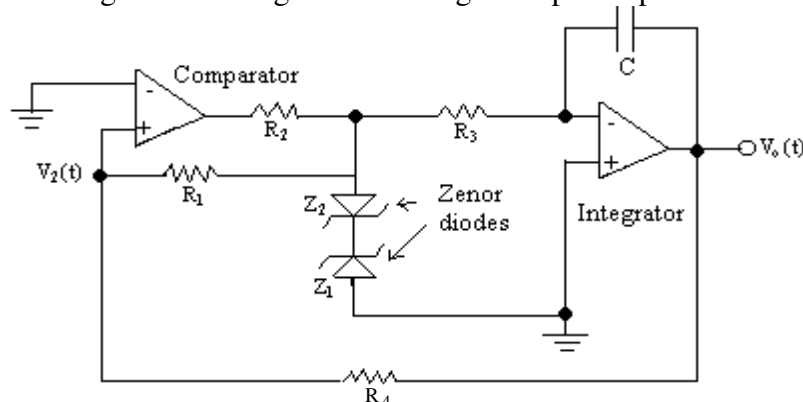
fig(3)

During the time the MOSFET is ON, the V_i appears across the capacitor and so at the output of the non-inverting amplifier as V_o . When MOSFET is off during T_{OFF} , the input is isolated from C and the op-amp circuit. During this time, the voltage on C will be held constant at a value of V_i , which prevailed at the end of T_{ON} . The T_{ON} is often called the 'sample period' and the T_{OFF} the 'hold period'. To obtain an output that closely approximates the input, the frequency of the control voltage at the gate should be as large as possible. To retain the sampled voltage without loss, the capacitor should be of very good quality with the least charge leakage.

Q.99 Write a neat circuit diagram of saw-tooth wave generator using op-amps and describe its operation. Derive an expression for the frequency of the wave. (10)

Ans:

The circuit of triangular – wave generator using two op – amps is shown in the figure below

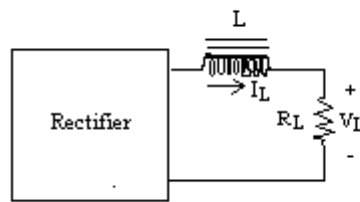


The operation of the circuit is explained with reference to the wave diagram shown below.

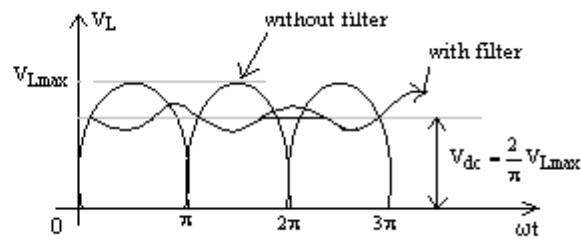
This is the simplest and the least expensive filter. A large value capacitor offers high impedance to d.c. Fig(3) shows how the capacitor helps in maintaining the load voltage as constant as possible. In the case of a full-wave rectifier without filter, the load voltage would also be the rectified waveform shown by the dotted line. But with C filter, the voltage across the load has much less ripple as shown by the full line trace.

(ii) Series Inductor filter:

Property of an inductor is to oppose any change in the current through it. An inductor can be connected to act as a filter between the load and a basic rectifier as shown in fig(4).



fig(4)

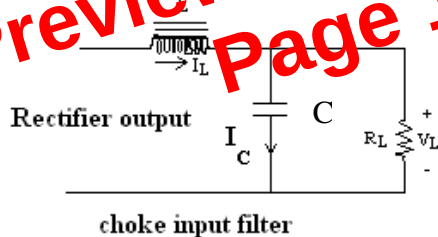


fig(5)

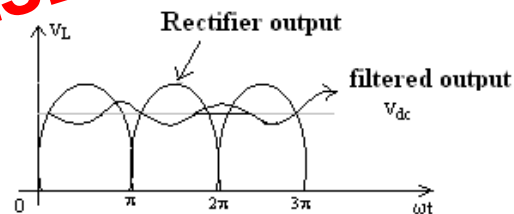
The inductor or choke stores energy in its magnetic field when the current is above an average value. The stored energy is released when the load current falls below the average value. The effect of the inductor filter is illustrated in fig 5 above.

(iii) Choke Input filter (L-Section filter):

As explained above in connection with inductor filter and capacitor filter, while capacitor acts to keep the voltage across itself constant and inductor acts to keep the current through it constant, the advantages of the properties of both an inductor and a capacitor are combined into an L-Section filter shown in fig 6.



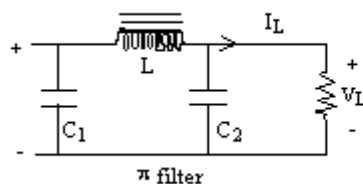
fig(6)



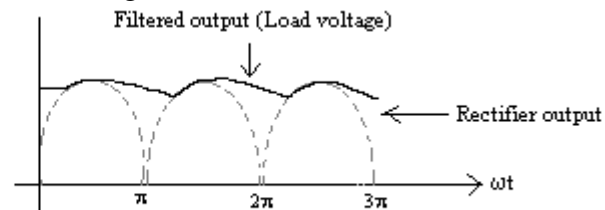
fig(7)

The effect of the L-Section filter is illustrated in fig 7. This provides d.c. output more ripple free than either C-filter alone or choke filter alone.

(iv) π -filter: The circuit of π -filter is shown in fig 8.



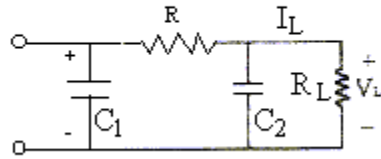
fig(8)



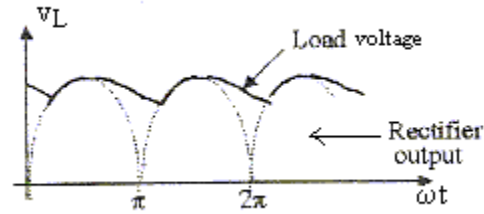
fig(9)

Because of the additional capacitor at the input of the filter, the d.c. output is of a higher value and more ripple-free than is possible by any of the filters discussed earlier. The effect of the filter on a full-wave rectifier output is illustrated in fig 9.

(v) **RC-Filter:** The RC filter circuit is shown in fig 10.



fig(10)



fig(11)

The disadvantages of the π -filter are its bulk, weight and higher cost. In place of L, if resistor R is used, the effect is almost similar to that obtained from π -filter. However, the R being dissipative of energy, the overall efficiency of the power supply will be less than possible with π -section filter. Also the ripple factor in this case would be poorer than in a π -section filter where an inductor is used.

Q.102 Delineate the concept of 'duality' in Boolean algebra. (3)

Ans:

It is the property of Boolean algebra that for a given Boolean expression there always exists a dual. Stated succinctly,

Two Boolean { Functions
Expressions
maps } will be called "duals" if they differ only by the simultaneous

interchange of AND for OR and "0" for "1"

All postulates, theorems and axioms of Boolean algebra are to be stated in pairs, one statement being the dual of the other statement.

e.g.: The expression $x + xy = x$ which is law of absorption has a dual $x(x + y) = x$.

Dual logic tables:

Table for 'OR'

x	y	$x+y$
0	0	0
0	1	1
1	0	1
1	1	1

If the '1' are replaced by '0'
we get the table for AND as
shown on right side

Table for 'AND'

x	y	$x.y$
1	1	1
0	0	0
1	0	0
0	1	0