

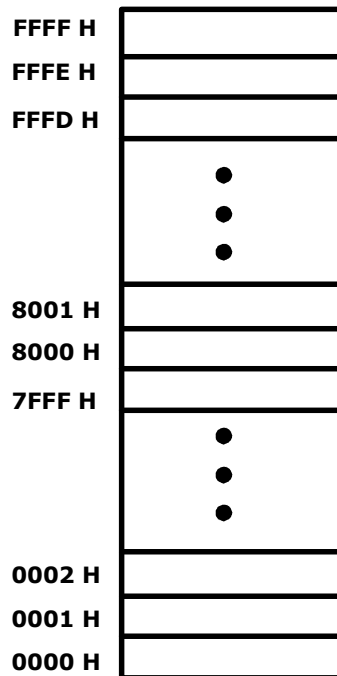


Figure 3.1: 64KB Memory Map
(Single Block)

Instead of connecting all the 16 address lines to a single 64 KB memory device, we can also use memory devices of lower capacity. In such cases the physical memory space of the microprocessor is divided into smaller memory spaces or memory blocks. Each block is selected by a block select address signal and the memory locations within a block are accessed by the processor's address lines. This is called address portioning. For example if the memory device (memory block) has only 13 address lines, we can use the lower 13 address lines ($A_0 - A_{12}$) to access the locations within a memory block and the remaining 3 lines (A_{13} , A_{14} and A_{15}) to access 8 such blocks. These three lines are called the **block select address signals** and this is called **address partitioning**. Depending on the number of memory blocks, the number of block select address lines will change. The starting address and ending address of each block can be found as shown in Table 3.2. Since each block is an Integrated Chip (IC), and each chip has a **Chip Select** signal, the block select address lines must be used to select the ICs. We have to produce eight chip select signals from the three address lines. Therefore we have to decode these lines using a 3 to 8 decoder or 1 of 8 decoder. In this case the lower thirteen address lines of the processor are connected to the 13 address lines of the memory chip and hence they are internally decoded in the memory. The higher 3 address lines (A_{13} , A_{14} and A_{15}) are externally decoded by a 3 to 8 decoder. Since three lines can provide a maximum of 8 addresses, in this case they are said to be fully decoded and hence each location in each block has a specific unique address as shown in table 3.2. This is called as absolute address decoding. The diagrammatic representation of each block with its address range shown in figure 3.2 is called the memory map of the microprocessor system.

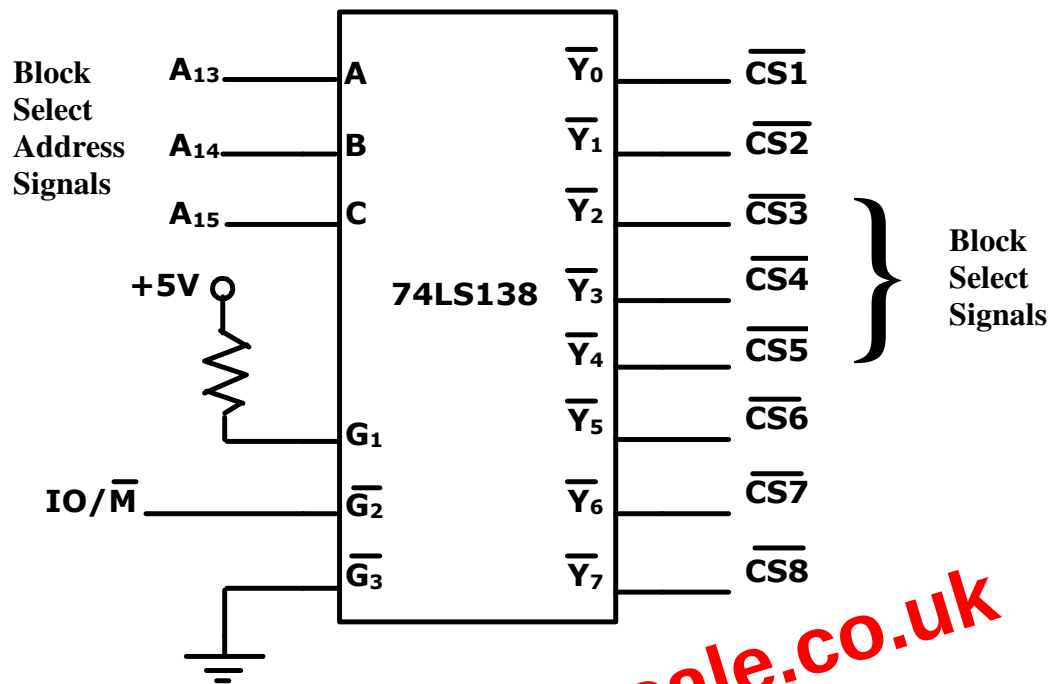


Figure 3.3 Memory Block Decode

In this type of memory interfacing, all the address lines (A_0 to A_{15}) have been used. Each location in the memory will have a single address. This type of address decoding is called as absolute or fully decoded addressing.

Most of the microprocessor based systems do not use the complete 64 KB memory space. Even one EPROM and a RAM will be sufficient. For example in the memory map shown in figure 3.2, if only the EPROM and RAM 2 are used in the practical system, the memory map of such a system can be given as shown in figure 3.5. Still each location has single address. Therefore it is also called absolute address decoding. The main advantage of this type of decoding is, you can add memory devices for this system without disturbing the already connected devices. The memory interface diagram for this case is given in figure 3.6.

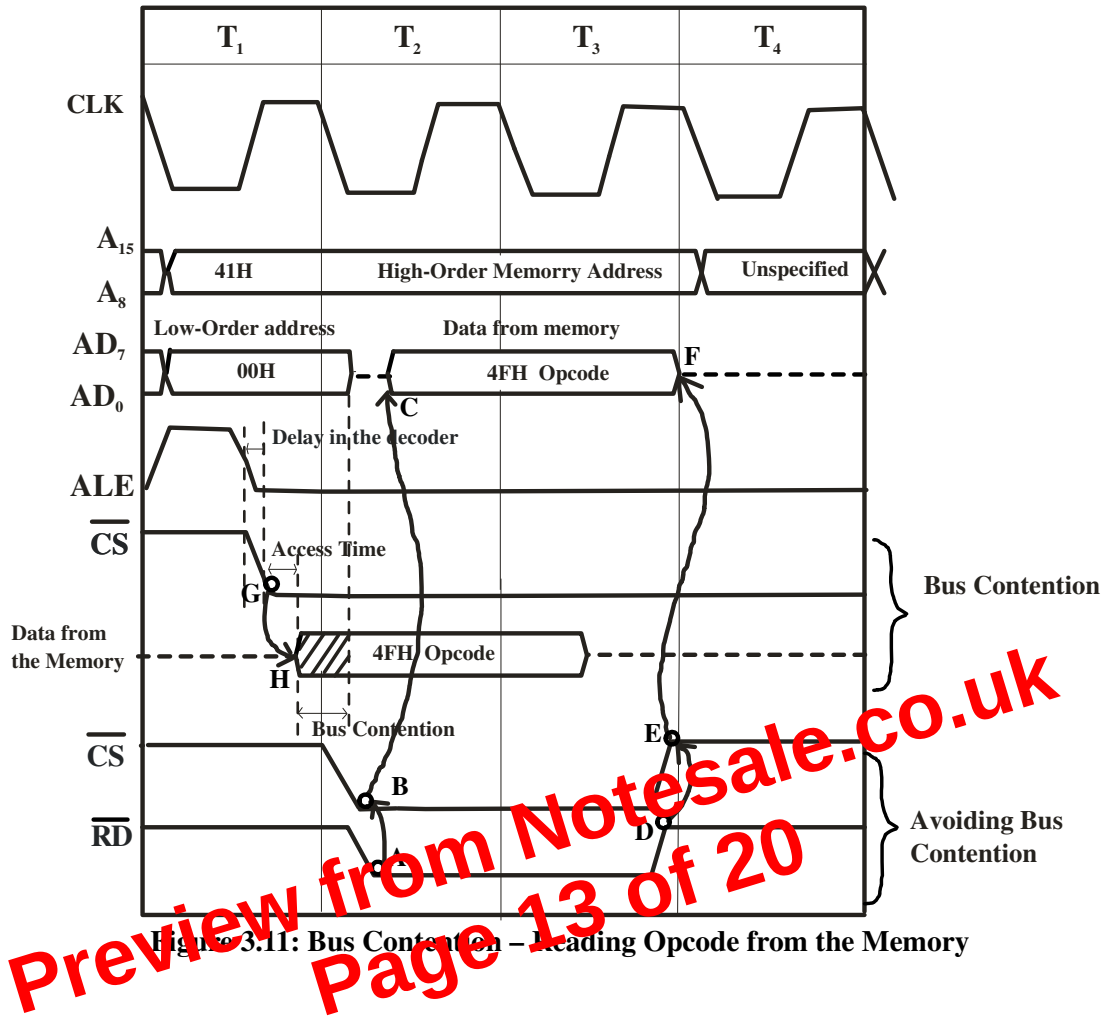


Figure 3.11: Bus Contention – Reading Opcode from the Memory