1 Logic Families (Task 1)

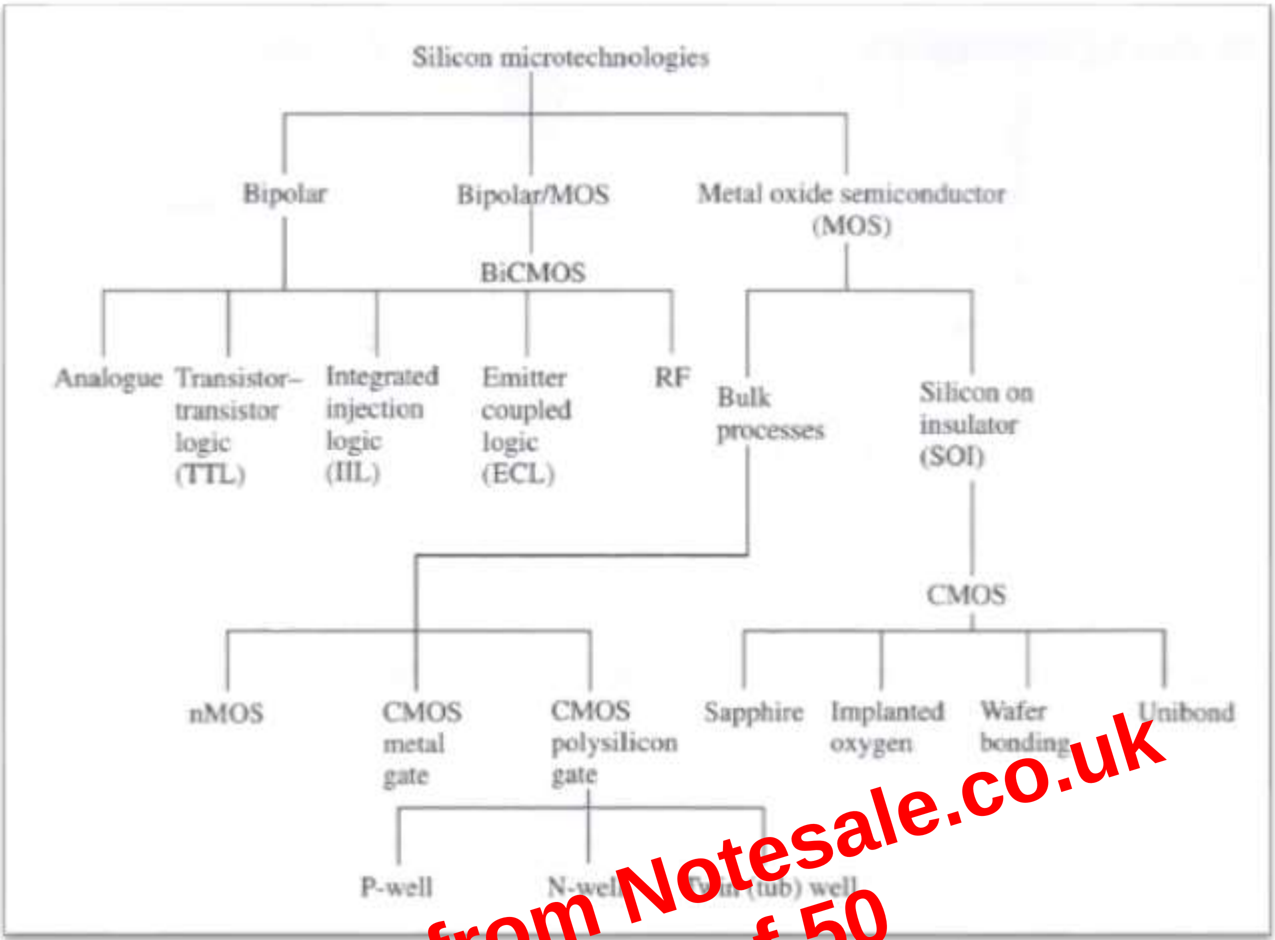

Figure 1: Different Logic Families (Nailis, 2014)

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Logic gates are built using transistors. The primary types used are:

- BJT (bipolar junction transistors)
- FET (field effect transistors) especially Metal-Oxide Semiconductors (MOSFET)
  MOSFETs are either: NMOS or PMOS

The TTL family of logic gates is created by connecting bipolar junction transistors.

The CMOS family of logic gates is created by connecting NMOS and PMOS transistors.

1.2 Complementary Metal-Oxide-Semiconductor (CMOS)

Table 2: CMOS chip families

Chip family	Description	Acronym
4000	Original CMOS	
40H00	High Speed CMOS (Slower than LS TTL)	
74C00	CMOS. Pin compatible with TTL Lower power, but still slower	
74HC00	CMOS. Pin compatible. Less power. Greater noise immunity. Increased temperature operating range	

1.3 TTL vs CMOS

Table 3: Advantages and disadvantages of TTL and CMOS

Family	Advantages	Disadvantages
TTL	More robust – less susceptible to static damage	Uses more power than CMOS
CMOS	Lowest power consumption Most common logic family today Used in all PC processor chips	Susceptible to damage by static and voltage spikes

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2 TTL and CMOS Interoperability

2.1 TTL Driving CMOS

(I.e. TTL output to CMOS input.)

2.1.1 Voltage Comparison

Table 6: TTL o/p to CMOS i/p - voltage comparison

TTL Output			CMOS Input		Comments
Series	$V_{OH(MIN)}$		$V_{IH(MIN)}$	Series	
		5.0V			
		4.0V			
			3.85V	74AHC	Pull-up resistor required to use these CMOS devices.
			3.5V	4000/74HC/74AC	
		3.0V			
74ALS	2.7V				$V_{OH(MIN)} \geq V_{IH(MIN)}$ so the "1" voltage is compatible
74LS/74AS	2.5V				
74	2.4V				
		2.0V	2.0V	74HCT/74ACT/74AHCT	
			1.65V	74AHC	$V_{OL(MAX)} \leq V_{IL(MAX)}$ so the "0" voltage is compatible
			1.5V	4000B/74AC	
		1.0V	1.0V	74HC	
			0.8V	74HCT/74ACT/74AHCT	
74LS/74AS/74ALS	0.5V				
74	0.4V				
		0.0V			
Series	$V_{OL(MAX)}$		$V_{IL(MAX)}$	Series	
TTL Output			CMOS Input		Comments

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As Table 6 shows all the TTL chips are voltage compatible with most of the CMOS chips. In order to use 4000, 74HC, 74AC and 74AHC CMOS chips we must use a pull-up resistor (see Figure 4).

2.2.3 Fan-Out

Table 11: Fan-out CMOS driving TTL – High level "1"

$$\text{"1"}\ N = \frac{CMOS\ I_{OH(max)}}{TTL\ I_{IH(max)}}$$

			TTL				
			74	74F	74AS	74LS	74ALS
		µA	40	20	20	20	20
		mA	0.04	0.02	0.02	0.02	0.02
CMOS	74AC/74ACT	24	600	1200	1200	1200	1200
	74AHC/74AHCT	8	200	400	400	400	400
	74HC/74HCT	4	100	200	200	200	200
	4000B	0.4	10	20	20	20	20

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Table 12: Fan-out CMOS driving TTL– High level "0"

$$\text{"0"}\ N = \frac{CMOS\ I_{OL(max)}}{TTL\ I_{IL(max)}}$$

			TTL				
			74	74F	74AS	74LS	74ALS
		mA	1.6	0.6	0.5	0.4	0.1
CMOS	74AC/74ACT	24	15	40	48	60	240
	74AHC/74AHCT	8	5	13	16	20	80
	74HC/74HCT	4	2	6	8	10	40
	4000B	0.4	0	0	0	1	4

The smaller of the two corresponding values (see Table 11 and Table 12), gives the Fan-out for each pairing (so only need to look at Table 12).

Note: 4000B CMOS chip cannot directly drive any of the following TTL chips: 74, 74F, 74AS.

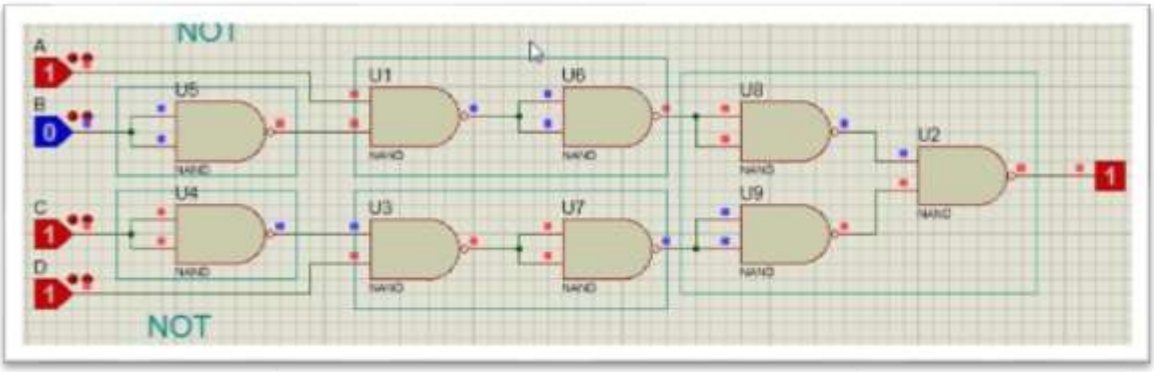

Figure 35: I/P '1011' O/P '1'

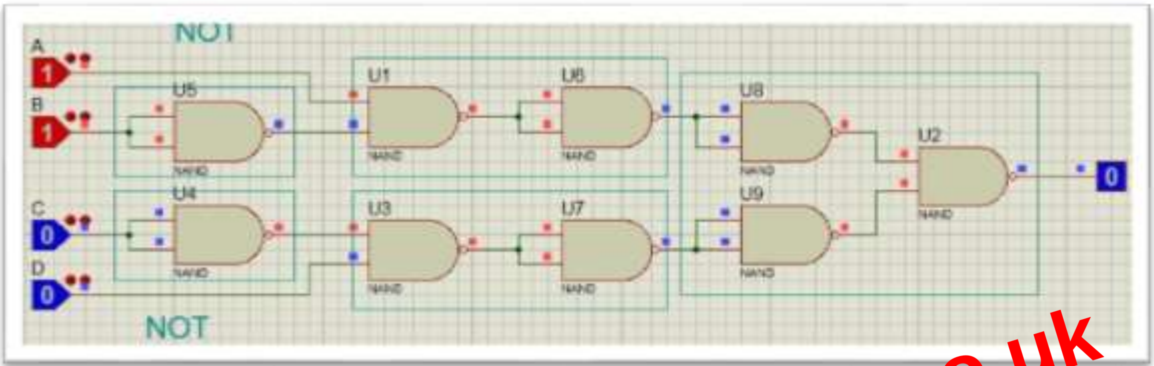

Figure 36: I/P '1100' O/P '0'

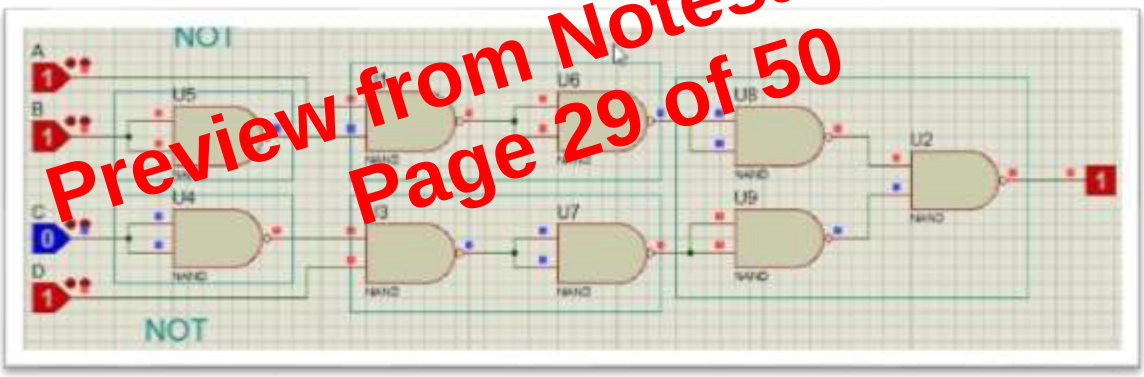

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Figure 37: I/P '1101' O/P '1'

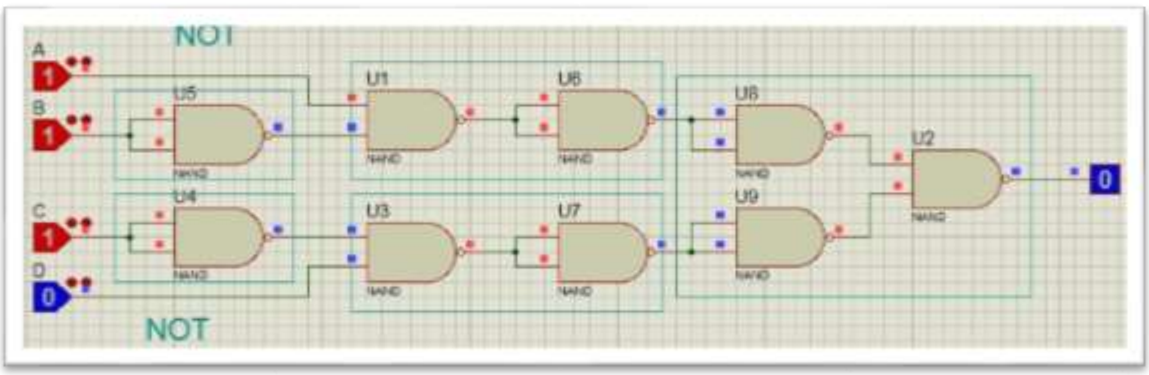

Figure 38: I/P '1110' O/P '0'

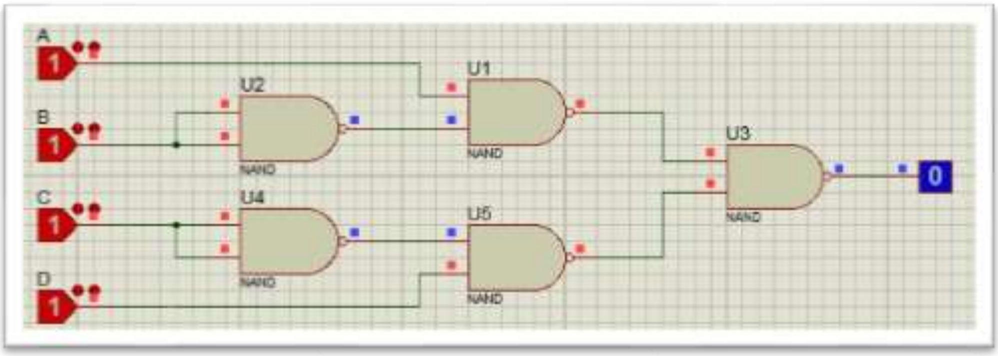

Figure 55: I/P '1111' O/P '0'

3.4 Why NAND Only Logic?

The output from the three circuits (Figure 8, Figure 24 and Figure 40) is the same for each input combination. The change to NAND-only logic has not affected the output of the circuit. The optimisation to the circuit, similarly, has not affected the output.

The originally circuit used 3 different types of logic. As chips are only available with a single type of logic on them, the original circuit would require three chips to implement, assuming dual-AND, OR and dual-NOT.

The final circuit has five Boolean operators, the same as the original circuit, but now they are all the same type: NAND. Therefore this circuit can be implemented using a single chip, containing multiple NAND gates.

The cost of a logic chip is fairly standard, regardless of the type of gates contained. Three chips cost three times as much as one chip. (More if the additional wiring is taken into account.) Manufacturers making millions of boards will see a HUGE saving in costs, reduced board size, and lower power consumption. Placing three chips on a board takes three times as long as placing one chip (even if a robot is doing it). As time is money, that's more profit.

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NOR only circuits can also be used with similar results.

Figure 74 shows the timing of the circuit. Starting from the top:

- A signal generator produces pulses that are connected to the clock (*CLK*) input of *U1:A*. Notice U1A goes high as clock pulse 1 goes from high to low.
- When *U1:A* goes from high to low (at the end of clock pulse 2), *U1:B* goes high.
- When *U1:B* goes from high to low (at the end of clock pulse 4), *U2:A* goes high.
- When *U2:A* goes from high to low (at the end of clock pulse 8), *U2:B* goes high.
- At the end of clock pulse 16 the count starts over.

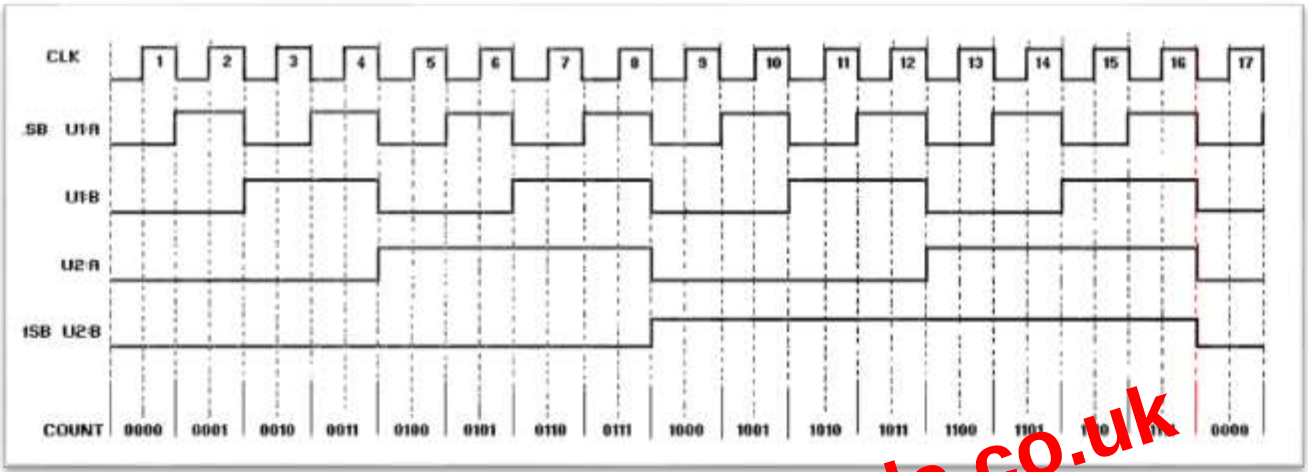

Figure 74 Timing diagram for 0-15 Ripple Counter. Adapted from (Tangient LLC, 2014)

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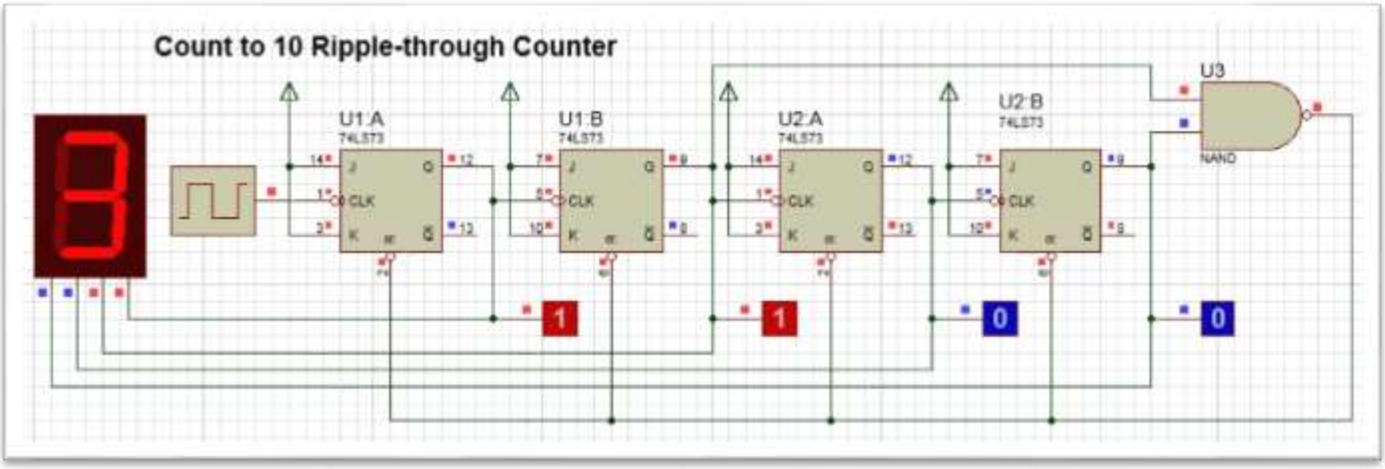

Figure 78: LSB...MSB '1100' ==> '3'

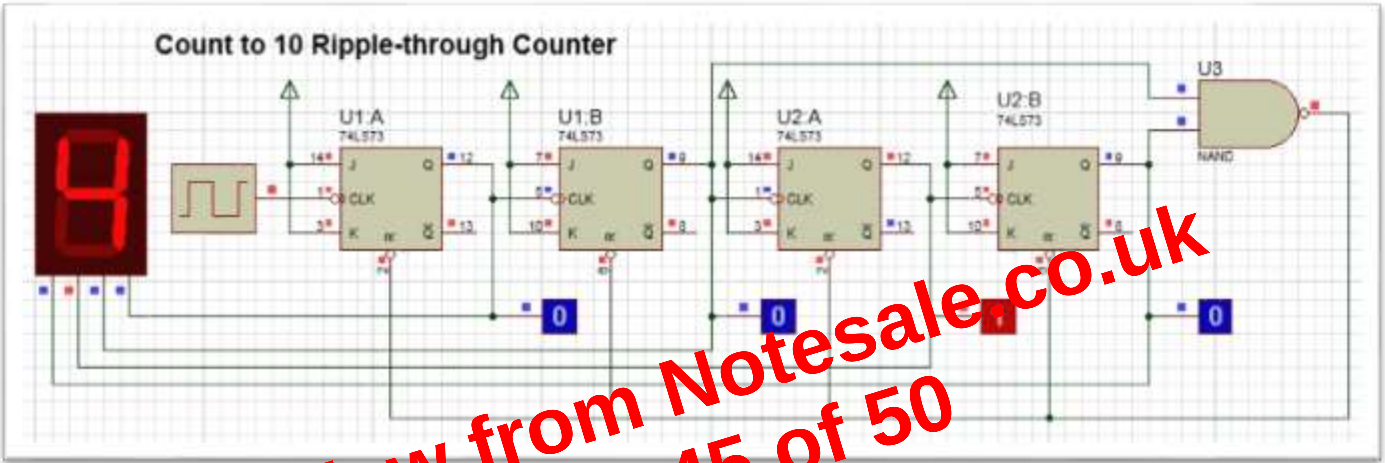

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Figure 79: LSB...MSB '0010' ==> '4'

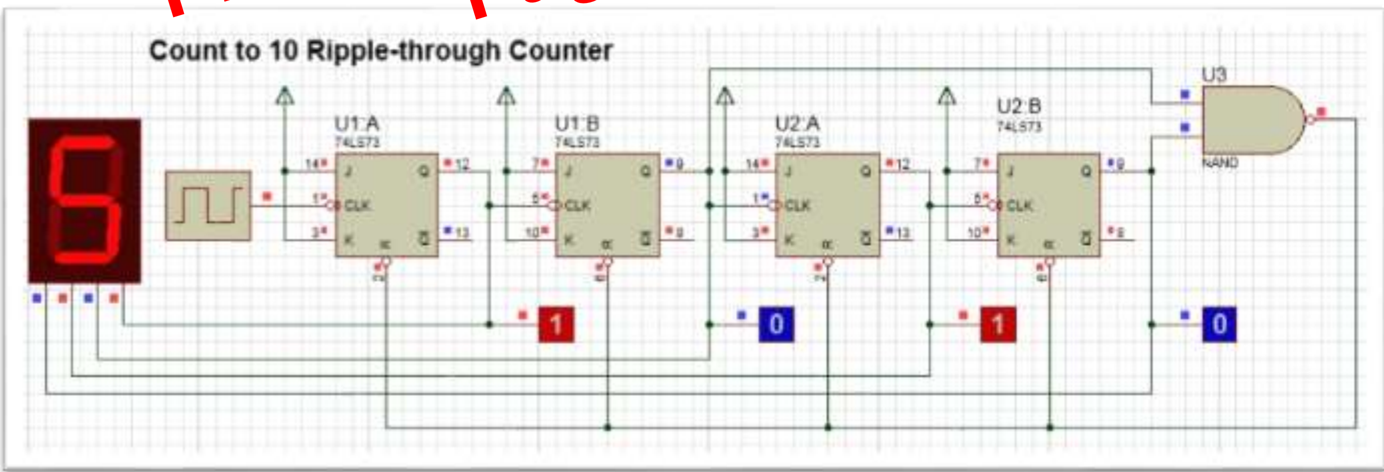

Figure 80: LSB...MSB '1010' ==> '5'