ECEN4827/5827 lecture notes

Effects of op-amp imperfections on application circuits (part 2)

Input offset voltage V_{OS}, input bias current I_B, and input offset current I_{OS}

Circuit example: *Analog integrator*

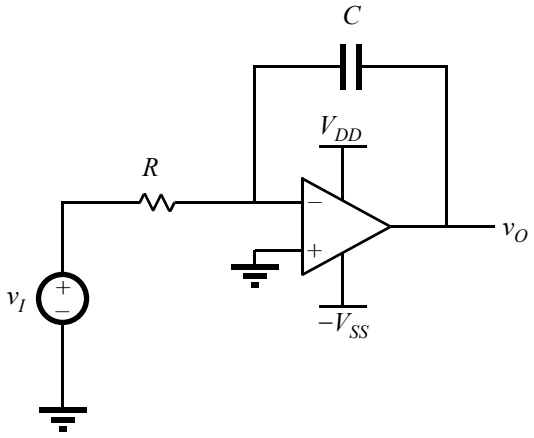

Figure 2.1: Analog integrator

Figure 2.1 shows an analog integrator circuit. Assuming an ideal op-amp, the closed-loop small-signal transfer function this circuit is:

$$(A_{CL})_{ideal}(s) = -\frac{1}{sCR} \ . \qquad (1)$$

The magnitude response of the ideal integrator is:

$$20\log\left|(A_{CL})_{ideal}(j\omega)\right| = 20\log\frac{1}{\omega CR} = -20\log(\omega CR) \ \text{[dB]}, \qquad (2)$$

the Bode plot of which is a straight line with a slope of –20 dB/decade. Note that the integrator gain tends to infinity as the signal frequency approaches zero (DC). As an exercise, derive an expression for the closed-loop transfer function $A_{CL}(s)$ of the circuit in Fig. 2.1 assuming the op-amp has a finite open-loop gain A_o.

The circuit analysis leading to (1) is based on the assumption that the op-amp operates with very large open-loop gain, *i.e.*, at a DC operating point away from the output saturation limits. In a practical analog integrator, however, the DC operating point in the circuit of Fig. 2.1 would (most likely) be at one of the saturation limits. To explain this, we need to introduce and examine another set of op-amp imperfections: the input offset voltage V_{OS}, the input bias current I_B, and input offset current I_{OS}.

Input offset voltage V_{OS}

In the circuit of Fig.2.2, with $v(+) = v(-) = 0$, the output voltage is ideally zero, $v_O = 0$. Due to unavoidable mismatches in the characteristics of the devices in the input differential stage of the op-amp (to be studied in more detail later when we discuss