Concepts

- Processor Registers and Instruction Execution
- Interrupts
- Memory hierarchy, Caching
- Input / Output
- Protection / Separation

Instruction Execution

- Fetched instruction is loaded into the Instruction Register (IR)
  - Processor interprets instruction in IR and performs one or more of the following actions
    - Data transfer:
      - Processor – Memory
      - Processor – I/O
    - Data processing: performing arithmetic / logic operations
    - Control: an instruction may specify that the sequence of execution to be altered (comparable to an “If-then” or ”go-to” statement)

Interrupt Handling

- Interrupts transfer control to an interrupt handler (also called "Interrupt Service Routine")
  - When an interrupt occurs, processor "jumps" to an interrupt handler
- An interrupt handler is program code that manages such an interrupt, is part of the overall operating system code

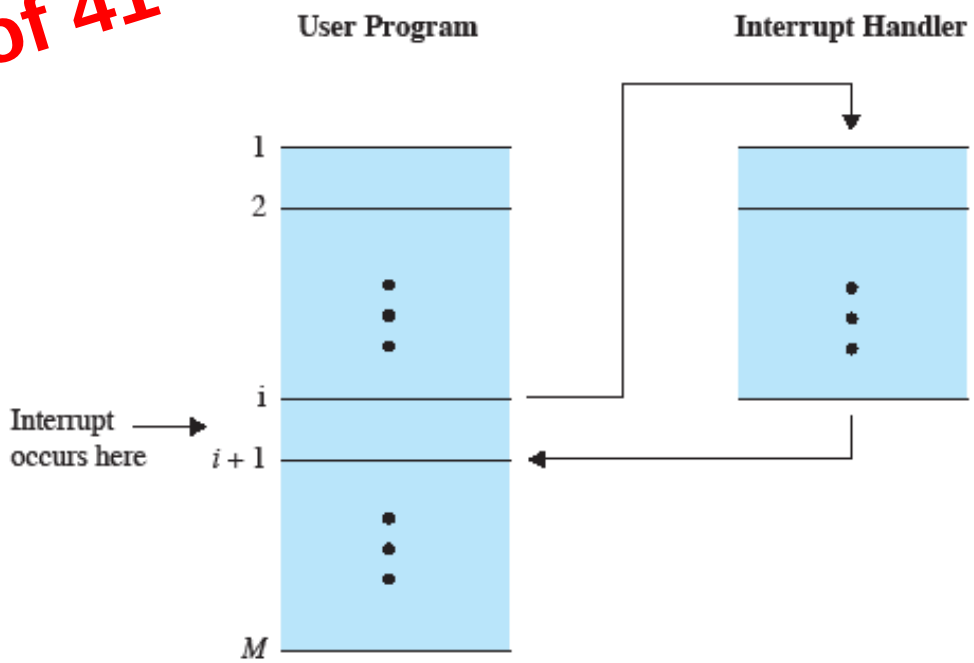
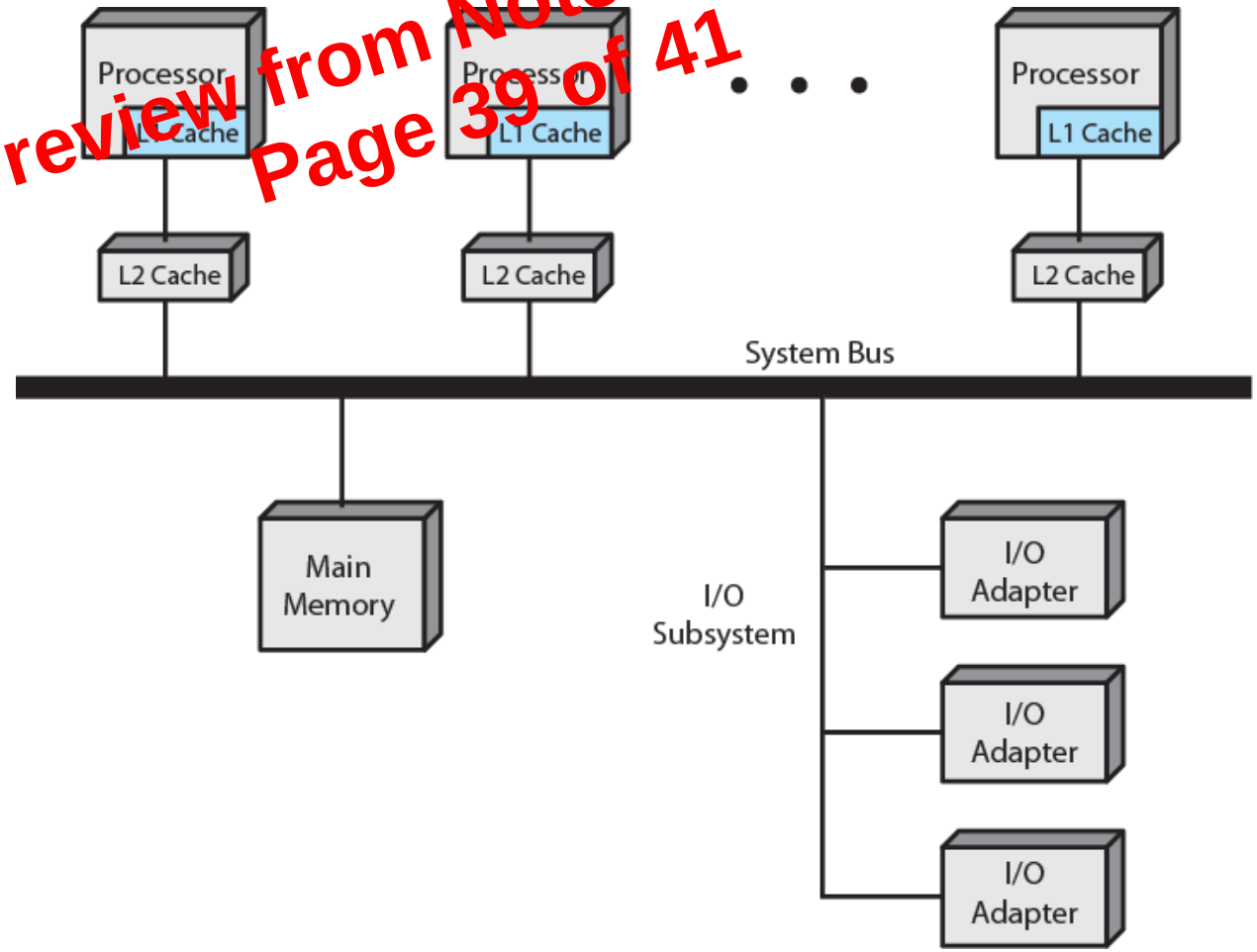


Figure 1.6 Transfer of Control via Interrupts

Cache Memory

- Is a hardware feature
  - Cache contains a copy of a portion of main memory
  - Processor first checks cache
  - If data not found in memory, another portion of main memory has to be copied into the cache
- Invisible to the operating system
- Utilises the “Principle of Locality”
  - Memory references by a processor tend to cluster
- Because of locality of reference, it is likely that many of the future memory references made by the processor will succeed with the current cache content

SMP Organisation



Multicore Systems

- A processor has multiple processing cores
  - Parallelism on the processor chip itself
  - Each core has all the components of a single processor
- Performance advantages
  - Multiple processors on a single chip brings huge performance advantages
  - Introduction of different levels of cache memory