A \ B	0	1
0	$\overline{A}.\overline{B}$	$\overline{A}.B$
1	$A.\overline{B}$	A.B

(a) 2-Variable

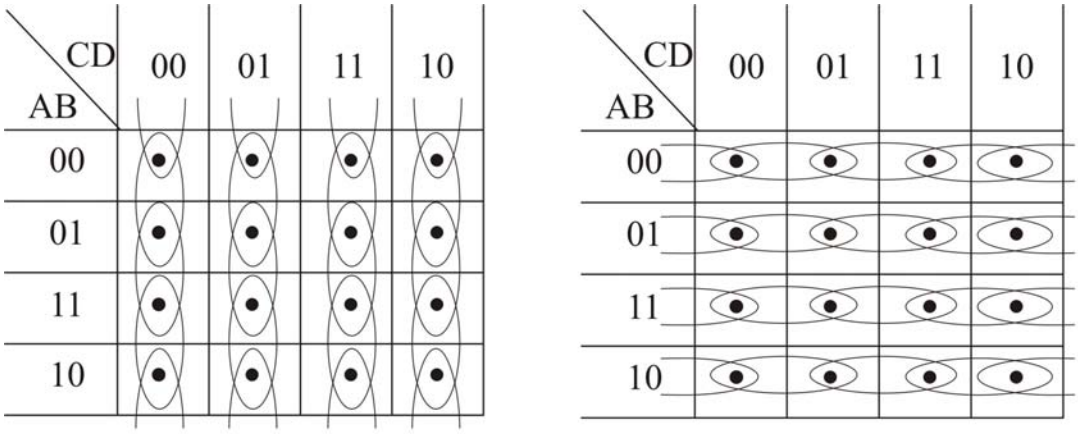
AB \ C	0	1
00	$\overline{A}.\overline{B}.\overline{C}$	$\overline{A}.\overline{B}.C$
01	$\overline{A}.B.\overline{C}$	$\overline{A}.B.C$
11	$A.B.\overline{C}$	A. B. C
10	$A.\overline{B}.\overline{C}$	$A.\overline{B}.C$

(b) 3-Variable

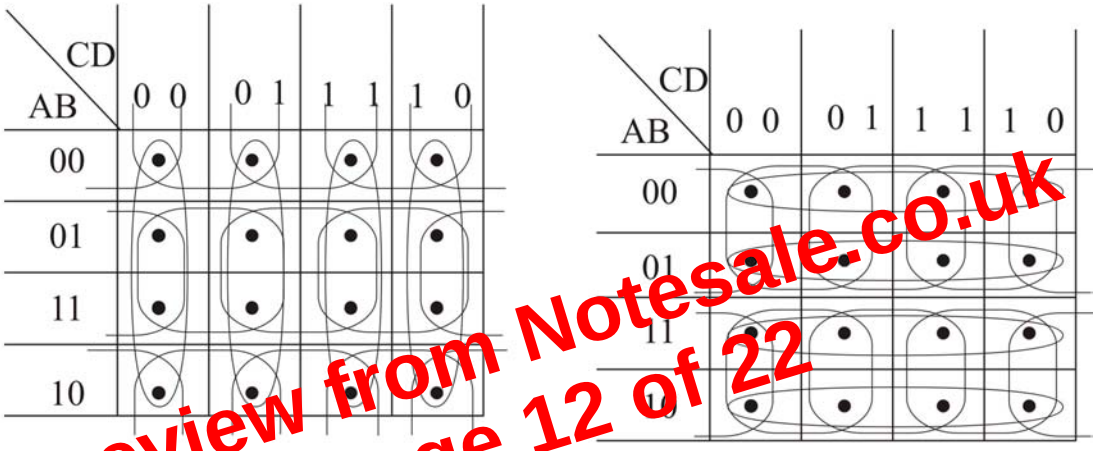
AB \ CD	00	01	11	10
00	$\overline{A}.\overline{B}.\overline{C}.\overline{D}.$	$\overline{A}.\overline{B}.\overline{C}.D.$	$\overline{A}.\overline{B}.C.D.$	$\overline{A}.\overline{B}.C.\overline{D}.$
01	$\overline{A}.B.\overline{C}.\overline{D}.$	$\overline{A}.B.\overline{C}.D.$	$\overline{A}.B.C.D.$	$\overline{A}.B.C.\overline{D}.$
11	$A.B.\overline{C}.\overline{D}.$	$A.B.\overline{C}.D.$	A.B.C.D.	$A.B.C.\overline{D}.$
10	$A.\overline{B}.\overline{C}.\overline{D}.$	$A.\overline{B}.\overline{C}.D.$	$A.\overline{B}.C.D.$	$A.\overline{B}.C.\overline{D}.$

(c) 4-Variable

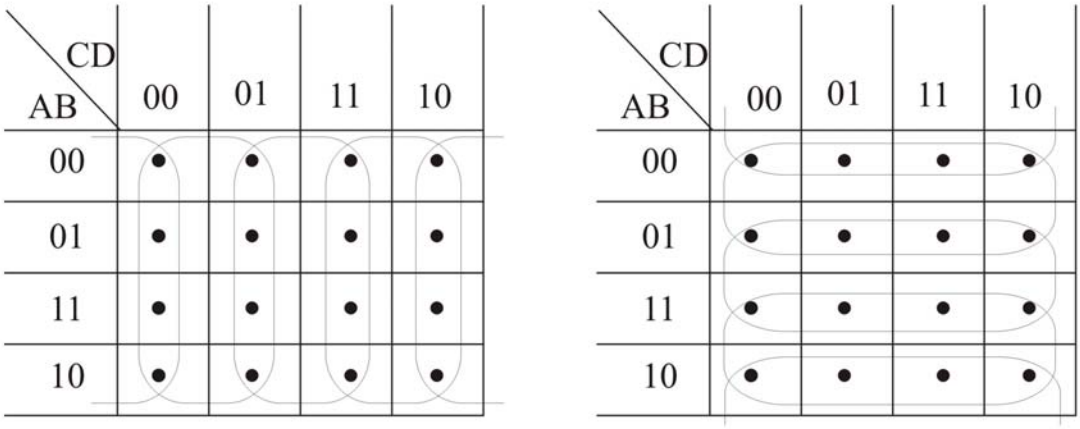
Fig. 12.5.1 K-map Configurations for n = 2, 3 & 4



(a) Binary Groups of 2 squares (32 possible groups)



(b) Binary Groups of 4 squares (24 possible groups)



(c) Binary Groups of 8 squares (8 possible groups)

Fig. 12.5.3. Possible Binary Groups in 4 Variable K-map

combinational logic problem, as the Boolean expression for any output variable can always be obtained in a minimal product of sums form.

As has been pointed out in Sec. 12.8, the cost of any circuit realisation is determined by the chip count, i.e. the number of IC chips required. A comparison of the four circuits given in Fig. 12.10.1 on this count shows that all of them require 2 chips – one for the three 2-input gates at the first (or input) level and the other for the 3-input gate at the second (or output) level. However, one should not generalise on the basis of this comparison that the four alternative circuit realisations always require the same chip count. Realisations based on a single inverting gate – NAND or NOR – will in general give lesser chip count than the AND-OR or OR-AND realisations, because of the possibility of sharing gates on the same chip at both levels of these configurations.

12.11 Circuits Using Multiplexers

Multiplexers can be used to obtain the circuit realisation of any given truth table as given in Sec. 12.9. Such a scheme requires a multiplexer with n-bit control i.e. a 2^n-input multiplexer, for an n-variable problem. The inputs to the multiplexers in this scheme are simply the '0' s and '1' s appearing is the corresponding entries in the truth table. A more practical scheme for realising any combinational logic with multiplexers is to generate inputs from one of the variables, using the remaining (n-1) variables as the control inputs. Clearly, the chip count would be reduced in this approach. The exact procedure for generating the necessary input from the K-map(s) pertaining to a given problem is outlined in Fig. 12.11.1, which depicts a 3-variable problem with A and B used as the control inputs of a 4-input multiplexer. The functional dependence of the inputs I_0, I_1, I_2 and I_3 on the variable C would be determined by the entries in the pairs of squares indicated by I_0, I_1, I_2 and I_3 respectively in the K-map. This is illustrated by the realisation of a Full Adder, having the K-maps given in Fig. 12.11.2. By simple inspection, one can write the following expressions for the inputs necessary for each of the two 4-input multiplexers – one giving SUM and the other giving CARRY as the output:

SUM MUX : $I_0 = C, I_1 = \overline{C}, I_2 = \overline{C}$ and $I_3 = C$,

CARRY MUX : $I_0 = O, I_1 = C, I_2 = C$ and $I_3 = 1$.

Thus if both C and $\overline{C}$ are available, a Full Adder can be realised by a dual 4-input multiplexer, resulting in half the chip count in comparison with a realisation using 8-input multiplexers.